Features

- Constant frequency or constant off-time operation
- Switch mode controller for single switch drivers: Buck/Boost/Buck-boost/SEPIC
- Closed loop control of output current
- Internal 450V linear regulator (can be extended using external zener diodes)
- Internal 2% Voltage Reference
- High PWM dimming ratio
- Programmable MOSFET current limit
- Programmable slope compensation
- Output short circuit protection
- Enable & PWM dimming
- Soft start
- +0.2A/-0.4A GATE drive

Applications

- RGB backlight applications
- Automotive LED driver application
- Battery Powered LED lamps

General Description

LD7103 is a current mode control LED driver IC. It has been designed for the purpose of controlling single switch PWM converters (buck, boost, buck-boost, or SEPIC) at a fixed frequency or fixed off-time mode.

A peak current control scheme is used by the controller (with programmable slope compensation). It includes an internal trans-conductance amplifier to modify the output current in closed loop. This allows high output current accuracy.

Programmable MOSFET current limit allows for current limiting during input under voltage and output overload conditions.

For high power applications, the IC also comprises a 0.2A source and 0.4A sink GATE driver. There is an internal 9 to 450V linear regulator which powers the IC. This makes it no longer necessary to separate power supply for the IC. The LD7103 provides a TTL compatible, PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz.

The IC has the function of a NERR output which, can be used to disconnect LEDs in the circumstance that there is a NERR condition it will use an external disconnect FET.

The LD7103 based LED driver ideally suited to RGB backlight applications with DC inputs. The LD7103 based LED lamp drivers can reach efficiency of more than 90% for buck and boost applications.

Package Pin Out

1	HVIN	FB	14
2	VDD	ISET	13
3	GATE	CAP	12
	LD7103		
4	GND	DIM	11
5	CS	NERR	10
6	SLOP	VREF	9
7	RO	LD	8
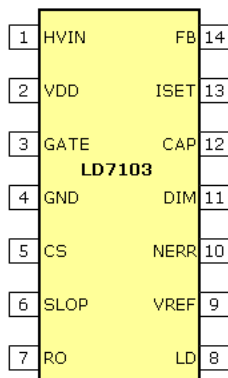
Ordering Information

Part No.	Package	Packing Options	
		Tube(TU)	Tape & Reel(TR)
LD7103	SOP-14	LD7103S2-TU	LD7103S2-TR

- Package material default is "Green" package.

Product Marking

LD8888
SSSSS…

●

✧ Line 1 – "LD" is a fixed character
8888: product name
✧ Line 2 – SSSSS…: lot number

Absolute Maximum Ratings

Parameter	Maximum	Unit
HVIN to GND	-0.5~ +450	V
VDD to GND	-0.3~ +13.5	V
CS to GND	-0.3~VDD+0.3	V
DIM to GND	-0.3~VDD+0.3	V
GATE to GND	-0.3~VDD+0.3	V
All other pins to GND	-0.3~VDD+0.3	V
Continuous Power Dissipation (T_A = +25°C)		
14-Pin SOIC, de-rate 10.0mW/°C above +25°C	1000	mW
Junction to ambient thermal impedance	82	°C/W
Operating ambient temperature range	-40~ +85	°C
Junction temperature	+125	°C
Storage temperature range	-65~ +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics

HVIN=24V, T_A=25°C unless specified, otherwise minimum and maximum values are guaranteed by production testing requirements.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input						
Input DC supply voltage range	V_{INDC}	DC input voltage	9[1]	–	450	V
Shut-down mode supply current	I_{INSD}	DIM connected to GND, HVIN = 24V	–	1.0	1.5	mA
Internal Regulator						
Internally regulated voltage	VDD	HVIN = 9~450V, IDD(ext) = 0, DIM= GND	7.25	7.75	8.25	V
VDD under voltage lockout threshold	UVLO	VDD rising	6.20	6.90	7.20	V
VDD under voltage lockout hysteresis	ΔUVLO	–	–	500	–	mV
Steady state external voltage that can be applied at the VDD pin[2]	VDD(ext)	–	–	–	12	V
Reference						
VREF pin voltage	V_{REF}	VREF bypassed with a 0.1µF capacitor to GND; ISET= 0; VDD = 7.75V; DIM = GND	1.225	1.25	1.275	V
Line regulation of reference voltage	$V_{REFLINE}$	VREF bypassed with a 0.1µF capacitor to GND; ISET = 0; VDD = 7.25 – 12V; DIM = GND	0	–	20	mV
Load regulation of reference voltage	$V_{REFLOAD}$	VREF bypassed with a 0.1µF capacitor to GND; ISET = 0-500µA; DIM = GND	0	–	20	mV
PWM Dimming						
DIM input low voltage	$V_{DIM(lo)}$	VDD = 7.25V – 12V	–	–	0.8	V
DIM input high voltage	$V_{DIM(hi)}$	VDD = 7.25V – 12V	2.0	–	–	V
DIM pull-down resistance	R_{DIM}	V_{DIM} = 5.0V	50	100	150	KΩ

Notes:
1. See application section for minimum input voltage
2. Parameters are not guaranteed to be within specifications if the external VDD voltage is greater than VDD(ext) or if VDD < 7.25V.

Electrical Characteristics (Continued)

HVIN=24V, T_A=25°C unless specified, otherwise minimum and maximum values are guaranteed by production testing requirements.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
GATE						
GATE short circuit current	I_{SOURCE}	V_{GATE} = 0V; VDD = 7.75V	0.2	–	–	A
GATE sinking current	I_{SINK}	V_{GATE} = 7.75V ; VDD = 7.75V	0.4	–	–	A
GATE output rise time	T_{RISE}	C_{GATE} = 1nF; VDD = 7.75V	–	50	85	ns
GATE output fall time	T_{FALL}	C_{GATE} = 1nF; VDD = 7.75V	–	25	45	ns
Current Sense						
Leading edge blanking	T_{BLANK}	–	100	–	600	ns
Delay to output of CAP comparator	T_{DELAY1}	CAP = VDD ; LD = VREF; V_{CS} = 0 to 600mV step	–	–	180	ns
Delay to output of LD comparator	T_{DELAY2}	CAP = VDD ; LD = 300mV ; V_{CS} = 0 to 400mV step	–	–	180	ns
Comparator offset voltage	V_{OFFSET}	–	0	–	50	mV
Oscillator						
Oscillator frequency	f_{OSC1}	RO = 1MΩ, HVIN<350VDC	71	80	90	
	f_{OSC2}	RO = 220KΩ, HVIN<250VDC	335	380	425	KHz
	f_{OSC3}	RO = 2MΩ, HVIN<450VDC	35	40	45	
Output Short Circuit						
Propagation time for short circuit detection	T_{OFF}	ISET = 200mV ; FB = 450mV; NERR goes from high to low	–	–	250	ns
NERR output rise time	$T_{RISE,NERR}$	1nF capacitor at NERR pin	–	–	300	ns
NERR output fall time	$T_{FALL,NERR}$	1nF capacitor at NERR pin	–	–	200	ns
Amplifier gain at ISET pin	G_{NERR}	ISET = 200mV	1.8	2	2.2	–
Soft Start						
Current into LD pin when pulled low	I_{LD}	NERR is low; 6.25KΩ between VREF and LD	–	–	200	µA
Slope Compensation						
Current sourced out of SLOP pin	I_{SLOPE}	–	0	–	100	µA
Internal current mirror ratio	G_{SLOPE}	I_{SLOPE} = 50µA ; $RC_{SENENSE}$ = 1KΩ	1.8	2	2.2	–

Pin Description

| Pin #	Name	Description
1	HVIN	This pin is the input of a 450V high voltage regulator.
2	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1uF).
3	GATE	This pin is the output GATE driver for an external N-channel power MOSFET.
4	GND	Ground return for all circuits. This pin must be connected to the return path from the input.
5	CS	This pin is used to sense the drain current of the external power FET. It includes a built-in 100ns (min) blanking time.
6	SLOP	Slope compensation for current sense. A resistor between SLOP and GND will program the slope compensation. In case of constant off-time mode of operation, slope compensation is unnecessary and the pin can be left open.
7	RO	This pin sets the frequency or the off-time of the power circuit. A resistor between RO and GND will program the circuit in constant frequency mode. A resistor between RO and GATE will program the circuit in a constant off-time mode.
8	LD	This pin provides a programmable input current limit for the converter. The current limit can be set by using a resistor divider from the VREF pin. Soft start can also be provided using this pin.
9	VREF	This pin provides 2% accurate reference voltage. It must be bypassed with at least a 10nF - 0.22µF capacitor to GND.
10	NERR	This pin is pulled to ground when there is an output short circuit condition or output over voltage condition. This pin can be used to drive an external MOSFET in the case of boost converters to disconnect the load from the source.
11	DIM	When this pin is pulled to GND (or left open), switching of the LD7103 is disabled. When an external TTL high level is applied to it, switching will resume.
12	CAP	Stable Closed loop control can be accomplished by connecting a compensation network between CAP and GND.
13	ISET	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the VREF pin.
14	FB	This pin provides output current feedback to the LD7103 by using a current sense resistor.

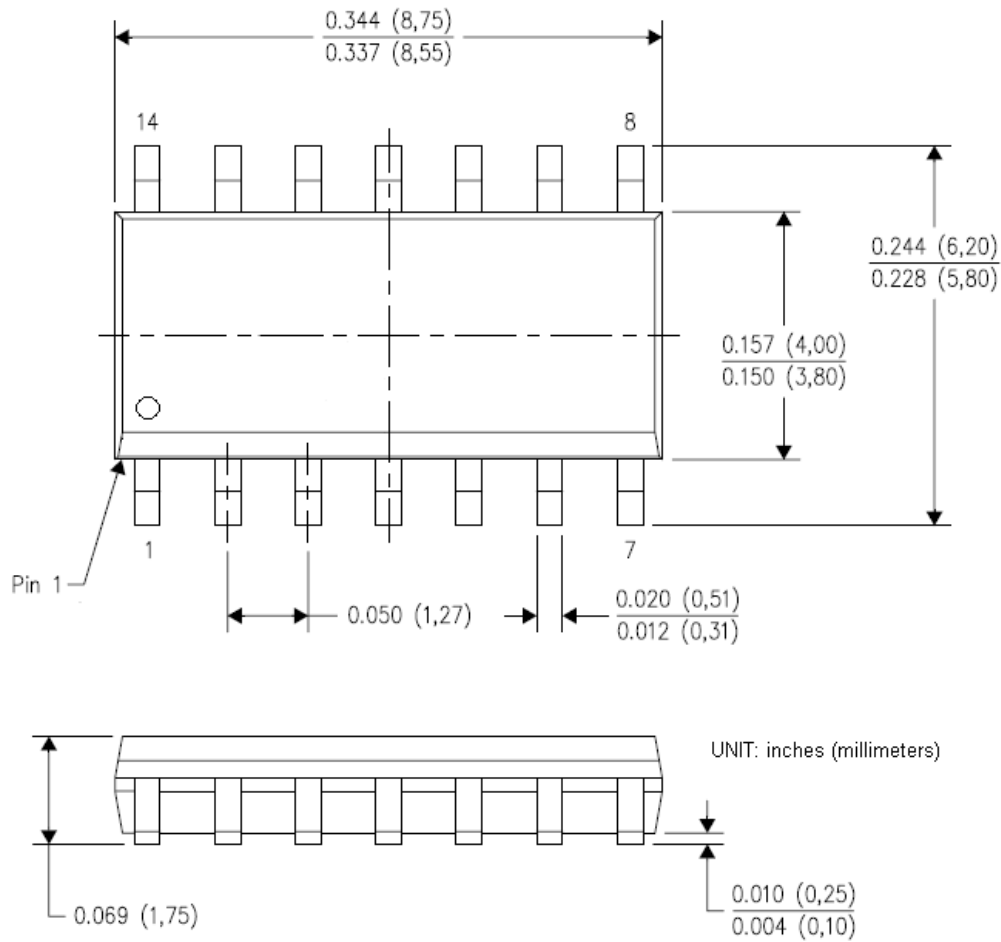## Functional Block Diagram
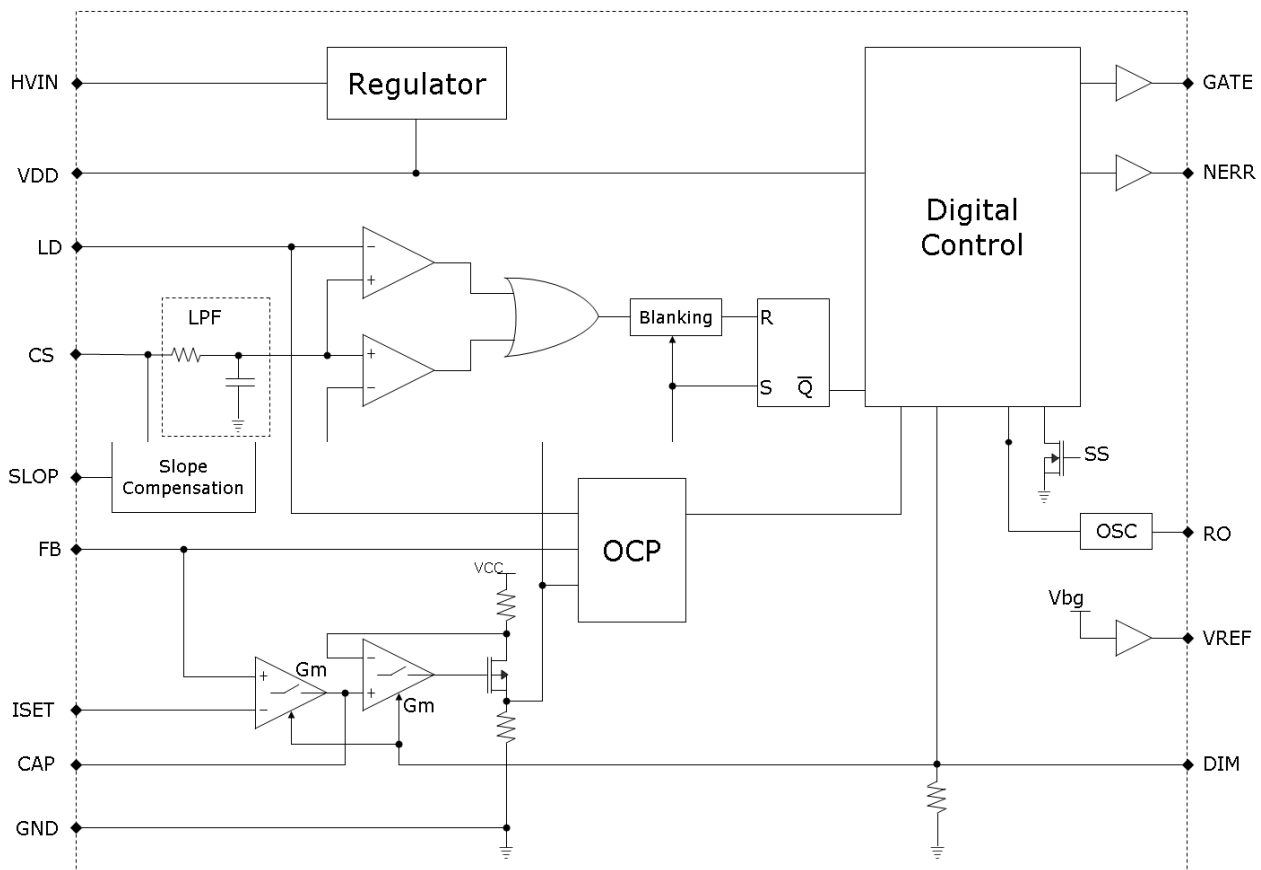
Typical Application Circuit – Boost
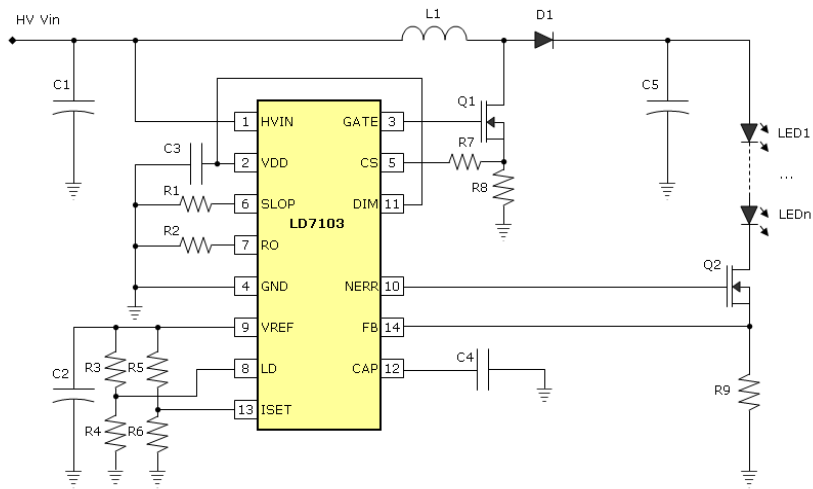
Typical Application Circuit – Buck
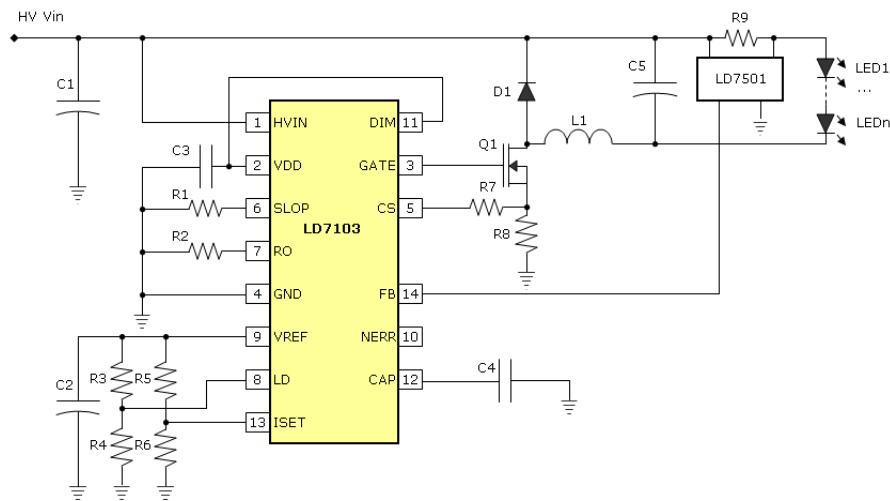
Typical Application Circuit – SEPIC
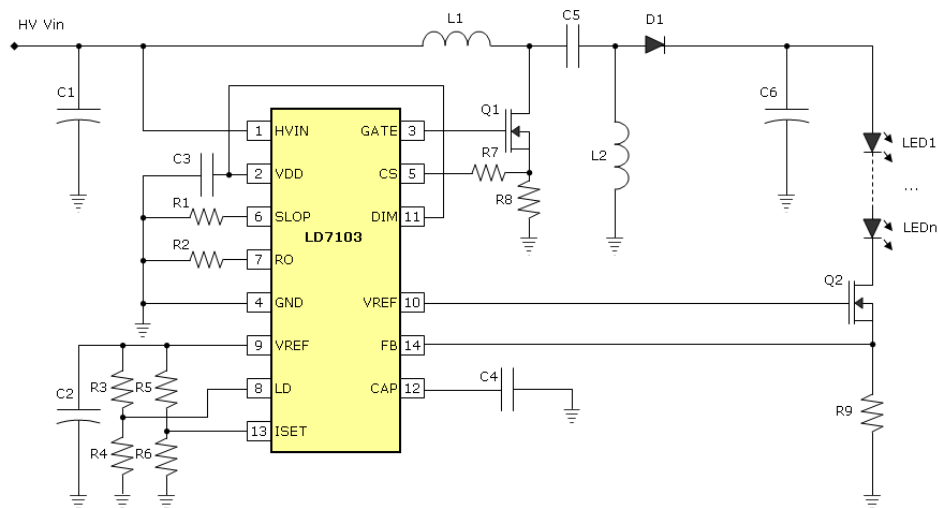
Package Outline
SOP-14:

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