Preliminary – **LD7002**

Power Factor Correction Controller

Features

- Optimized multiplier design for low total harmonic distortion (THD)
- Precise adjustable output over voltage protection
- Disable function for protection
- MOSFET over-current protection
- Zero current detector (ZCD)
- Under the universal input voltage
- 150μS internal startup time
- Under voltage lockout with 3V of Hysteresis
- Low (≤35μA) startup current
- Low (<1.7mA) operating current
- -800/+500mA totem pole gate drive with UVLO and high state clamp
- Advanced over current protection
- Patent pending

Applications

- LED bulb, T8 etc.
- LCD TV
- Adapter
- Ballast

General Description

The LD7002 is an efficient transition-mode power factor correction (PFC) controller. It detects the zero-current state and is the real zero current detector.

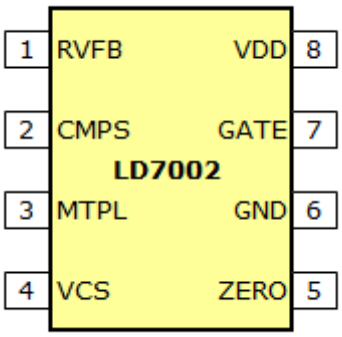
The LD7002 embedded with the ZCD, an optimized multiplier, and a special circuit, enable to reduce the AC input current distortion, and provides a low THD.

The LD7002 can be used under the input voltage of 110V or 220V, that is, can be used under the universal input voltage. It owns low consumption (≤35μA before start-up and <1.7mA running) and includes a disable function for IC remote ON/OFF.

With the features of the totem-pole output stage, capable of 800mA source and 500mA sink current, LD7002 is suitable for MOSFET drive and makes the device an excellent low-cost solution for LED bulb, T8, and LCD TV. The device also provides protection functions, such as, over voltage, over current, voltage lockout, and open loop protection.

The LD7002 especially provide an advanced over current protection function for the module.

Package Pin Out

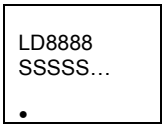


Ordering Information

		Packing Options	
Part No.	Package	Tube(TU)	Tape & Reel(TR)
LD7002	SOP-8	LD7002S1-TU	LD7002S1-TR

- Package material default is “Green” package.

Product Marking



- ✧ Line 1 – “LD” is a fixed character
  8888: product name
- ✧ Line 2 – SSSSS…: lot number

Absolute Maximum Ratings

Parameter	Maximum	Unit
VDD to GND	-0.3~ +30	V
VIN to GND	-0.3~ +8	V
GTE – IOH/IOL	±800	mA
Zero current detector current	+10/-50	mA
Continuous Power Dissipation (T_A = +25°C)		
8-Pin SOIC, de-rate 10.0mW/°C above +25°C	700	mW
Junction to ambient thermal impedance	120	°C/W
Operating ambient temperature range	-25~ +125	°C
Junction temperature	+150	°C
Storage temperature range	-55~ +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics

V_{DD}=12V, T_A=25°C unless specified, otherwise minimum and maximum values are guaranteed by production testing requirements.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Under Voltage Lockout						
Start threshold voltage	V_{THSTR}	V_{DD} increasing	10.5	11.5	12.5	V
Stop threshold voltage	V_{THSTP}	V_{DD} decreasing	–	8.5	–	V
UVLO Hysteresis	HY_{UVLO}		2.0	3.0	4.0	V
Zener voltage	V_Z	I_{DD} = 20mA	22	25	28	V
Supply Current						
Start up supply current	I_{SU}	V_{DD} = V_{THSTR} – 0.2V	20	60	100	µA
Static supply current	I_{DD}	Output no switching	–	3.0	6.0	mA
Operating supply current	I_{OP}	50KHz, C_L=1nF	–	4.0	8.0	mA
Operating supply current at OVP	I_{OVP}	V_{INV} = 3V	–	1.7	4.0	mA
Error Amplifier						
Voltage feedback input threshold	V_{THER}	T_A=25°C	2.465	2.500	2.535	V
		T_A=125°C	2.44	2.50	2.56	V
Line regulation	V_{LR}	V_{DD} = 14 ~ 25V	–	0.1	10.0	mV
Temperature regulation[*1]	V_{TR}	T_A=–25~125°C	–	20	–	mV
Input bias current	I_{BIN}	V_{INV} = 1 ~ 4 V	–0.5	–	0.5	µA
Output source current	I_{SRCER}	V_{INV} = V_{THER} – 0.1V	–2	–4	–	mA
Output sink current	I_{SNKER}	V_{INV} = V_{THER} + 0.1V	2	4	–	mA
Output upper clamp voltage[*1]	V_{CLMPU}	I_{SRCER} = 0.1mA	–	6.0	–	V
Output lower clamp voltage[*1]	V_{CLMPL}	I_{SNKER} = 0.1mA	–	2.25	–	V
Larger signal open loop gain[*1]	G_V		60	80	–	dB
Power supply rejection ratio[*1]	PSRR	V_{DD} = 14 ~ 25V	60	80	–	dB
Unit gain bandwidth[*1]	GBW		–	1.0	–	MHz
Slew rate[*1]	SR		–	0.6	–	V/µS

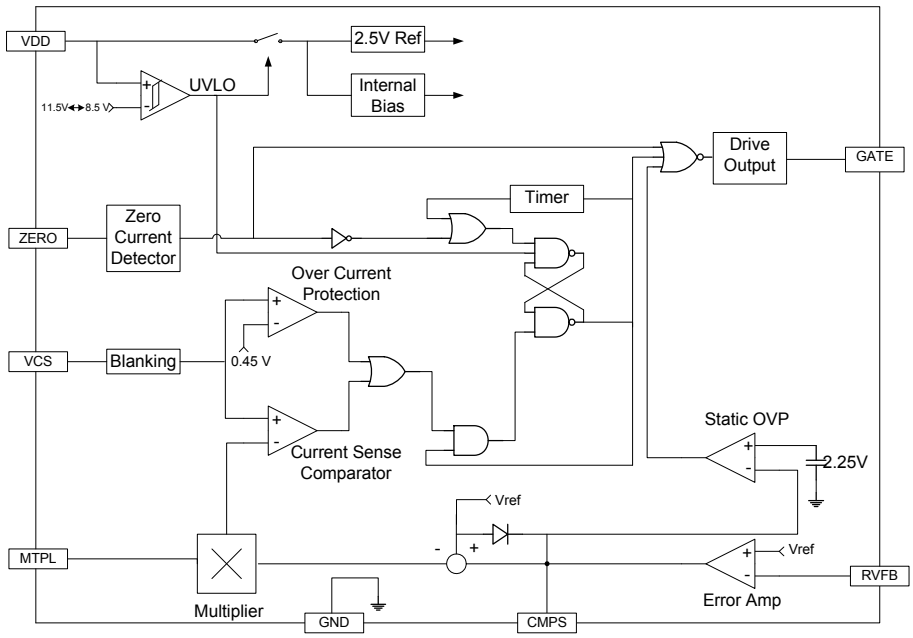
Multiplier						
MTPL input bias current	I_{BMTPL}		–0.5	–	0.5	μA
MTPL input voltage range	V_{MTPL}		0	–	3.8	V
CMPS input voltage range	V_{CMPS}		V_{REF}	–	V_{REF} +2.5	V
Multiplier gain[*1]	K	V_{MTPL} = 1V, V_{CMPS} = 3.5V	0.18	0.22	0.26	1/V
Maximum multiplier output voltage	$V_{MTPLMAX}$	V_{RVFB} = 0V, V_{MTPL} = 4V	1.65	1.80	1.95	V
Temperature Stability of K[*1]	ΔK/ΔT	T_A=–25~125°C	–	–0.2	–	%/°C
Current Sense						
Current sense input threshold[*1]	V_{CSTH}	V_{MTPL} = 0V, V_{CMPS} = 2.2V	–10	3	10	V
Current sense delay time[*1]	$T_{VCSDELAY}$		–	200	500	nS
Current limit reference voltage	V_{CS}		0.4	0.45	0.5	V
Zero Current Detection						
Input voltage threshold[*1]	V_{THZ}	V_{ZERO} increasing	1.7	2.0	2.3	V
Detect Hysteresis[*1]	HY_{ZERO}		0.2	0.5	0.8	V
Input clamp low voltage	V_{CLMPL}	I_{ZERO} = –100μA	0.45	0.75	1.00	V
Input clamp high voltage	V_{CLMPH}	I_{ZERO} = 3mA	6.5	7.2	7.9	V
Input bias current	I_{BZERR}	V_{ZERO} = 1 ~ 5 V	–1.0	–0.1	1.0	μA
Input H/L clamp diode current t[*1]	I_{CLAMP}		–3	–	3	mA
Gate Output						
Gate output high voltage	V_{GOH}	I_O = –10mA, T_A=25°C	10.5	11.0	–	V
Gate output low voltage	V_{GOL}	I_O = 10mA, T_A=25°C	–	0.8	1.0	V
Gate output rise time[*1]	T_{GORISE}	C_L=1nF	–	130	200	nS
Gate output fall time[*1]	T_{GOFALL}	C_L=1nF	–	50	120	nS
Maximum gate output voltage	V_{GOUVLO}	V_{DD} = 20V, I_O = 100μA	12	14	16	V
Gate output voltage under UVLO	V_{GOUVLO}	V_{DD} = 5V, I_O = 100μA	–	–	1	V
Restart						
Restart delay time	$T_{DELAYRST}$	V_{MTPL} = 1V, V_{CMPS} = 3.5V	–	500	–	μS
Over Voltage Protection						
Soft OVP detecting current	I_{SOVP}		25	30	35	μA
Dynamic OVP detecting current	I_{DOVP}		35	40	45	μA
Static OVP threshold voltage	V_{OVP}	V_{RVFB} = 2.7 V	–	0.8	–	V

Notes:
1. Guaranteed by design, not tested in production

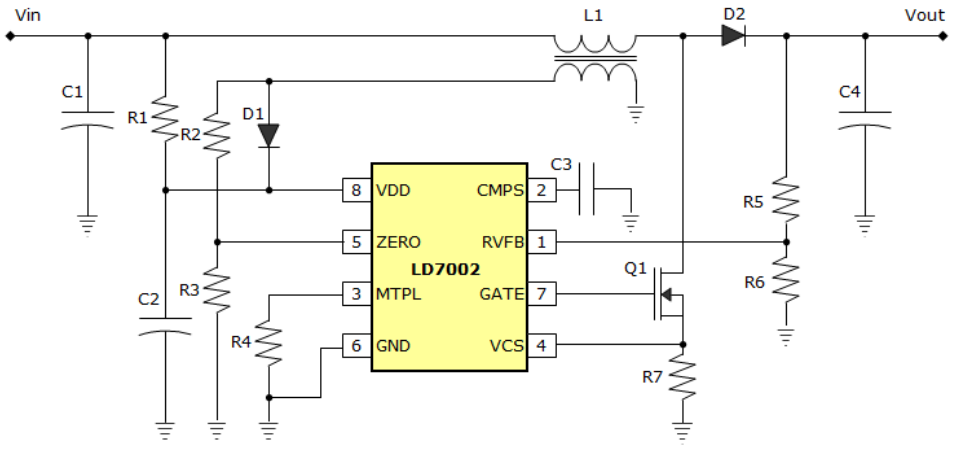
Pin Description

Pin #	Name	Description
1	RVFB	This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V
2	CMPS	This pin is the output of the trans-conductance error amplifier. Components for output voltage compensation should be connected between this pin and GND.
3	MTPL	This pin set the slope of the internal ramp. The voltage of this pin is maintained at 2.9V. If a resistor is connected between this pin and GND, current flows out of the pin and the slope of the internal ramp are proportional to this current.
4	VCS	This pin is the input of the over-current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise.
5	ZERO	This pin is the input of the zero current detection block. If the voltage of this pin goes higher than 1.5V, then goes lower than 1.4V, the MOSFET is turned on.
6	GND	This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
7	GATE	This pin is the gate drive output. The peak sourcing and sinking current levels are +500mA and -800mA respectively. For proper operation, the stray inductance in the gate driving path must be minimized.
8	VDD	This pin is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.

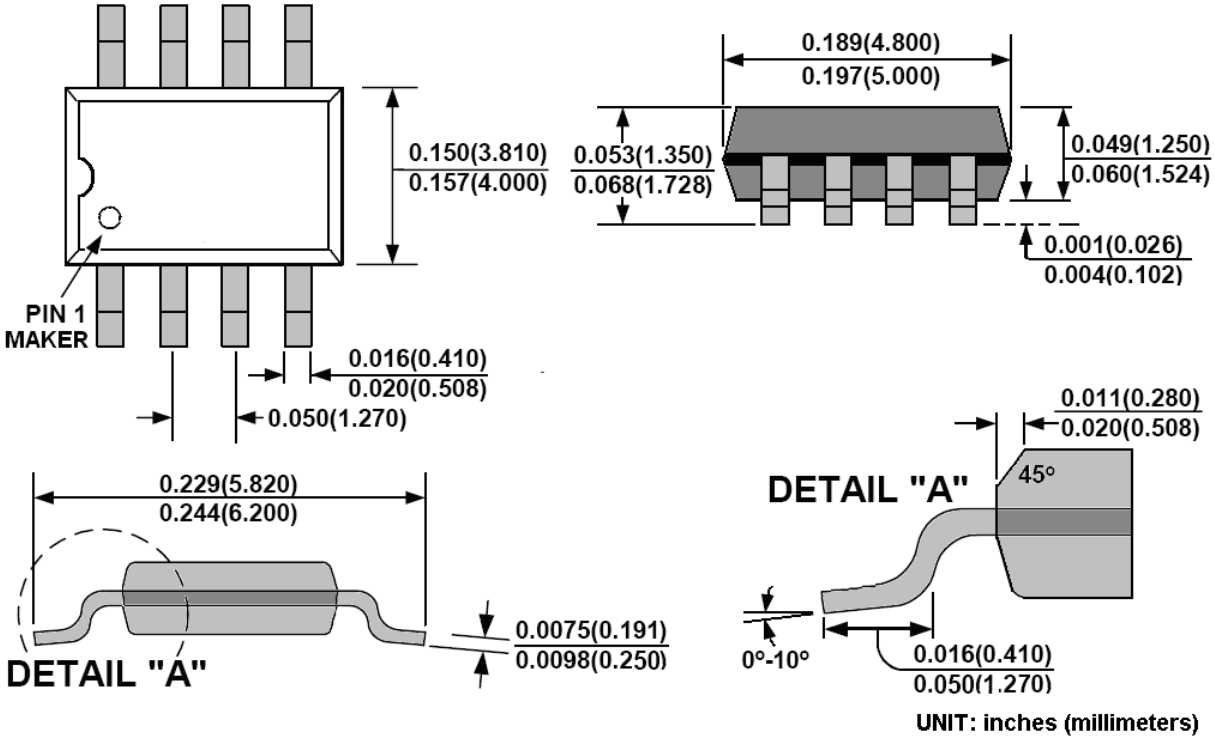
Functional Block Diagram



Typical Application Circuit



Package Outline



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