Features

- Low total harmonic distortion (THD)
- Precise adjustable output over voltage protection
- Open-feedback protection and disable function
- Zero current detector
- 150μS internal start-up timer
- MOSFET over-current protection
- Under voltage lockout with 3.5V Hysteresis
- Low start-up and operating current
- Totem pole output with high state clamp
- +500/-800mA peak gate drive current

Applications

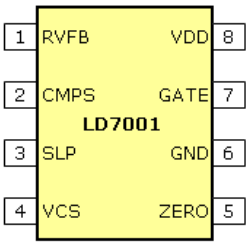
- Adapter
- Ballast
- LCD TV

General Description

LD7001 is the power factor correction (PFC) controller for boost PFC applications which operates in critical conduction mode. The voltage mode PWM comparing with internal ramp signal, then, provide error correction output to turn off MOSFET. This device has very low power loss of the input voltage for the operation.

By a know-how variable on-time control method, total harmonic distortion is lower than the conventional PFC. LD7001 provides many protections – over voltage, open feedback, over current, and under voltage lockout. It can be disabled by RVFB pin, with active low, which makes the operating current lower than 65μA.

Package Pin Out



Ordering Information

		Packing Options	
Part No.	Package	Tube(TU)	Tape & Reel(TR)
LD7001	SOP-8	LD7001S1-TU	LD7001S1-TR

- Package material default is “Green” package.

Product Marking

LD8888
SSSSS…
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- ✧ Line 1 – “LD” is a fixed character
  8888: product name
- ✧ Line 2 – SSSSS…: lot number

Absolute Maximum Ratings

Parameter	Maximum	Unit
VDD to GND	-0.3~ +16	V
VIN to GND	-0.3~ +6	V
GATE – IOH/IOL	+500/-800	mA
Output and detector clamping diodes	±10	mA
Continuous Power Dissipation (T_A = +25°C)		
8-Pin SOIC, de-rate 10.0mW/°C above +25°C	1000	mW
Junction to ambient thermal impedance	82	°C/W
Operating ambient temperature range	-40~ +125	°C
Junction temperature	+150	°C
Storage temperature range	-65~ +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics

V_{DD}=14V, T_A=25°C unless specified, otherwise minimum and maximum values are guaranteed by production testing requirements.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Under Voltage Lockout						
Start threshold voltage	V_{THSTR}	V_{DD} increasing	11	12	13	V
Stop threshold voltage	V_{THSTP}	V_{DD} decreasing	7.5	8.5	9.5	V
UVLO Hysteresis	HY_{UVLO}		3.0	3.5	4.0	V
Zener voltage	V_Z	I_{DD} = 20mA	20	22	24	V
Supply Current						
Start up supply current	I_{SU}	V_{DD} = V_{THSTR} – 0.2V	–	40	70	μA
Static supply current	I_{DD}	Output no switching	–	1.5	3.0	mA
Operating supply current	I_{OP}	50KHz, C_L=1nF	–	2.5	4.0	mA
Standby supply current	I_{SB}	V_{RVFB} = 0V	20	65	95	μA
Error Amplifier						
Voltage feedback input threshold	V_{THER}	T_A=25°C	2.465	2.500	2.535	V
Lin regulation	V_{LR}	V_{DD} = 14 ~ 20V	–	0.1	10.0	mV
Temperature regulation[*1]	V_{TR}		–	20	–	mV
Input bias current	I_{BIN}	V_{RVFB} = 1 ~ 4 V	–0.5	–	0.5	μA
Output source current	I_{SRCER}	V_{RVFB} = V_{THER} – 0.1V	–	–12	–	μA
Output sink current	I_{SNKER}	V_{RVFB} = V_{THER} + 0.1V	–	12	–	μA
Output upper clamp voltage	V_{CLMPU}	V_{RVFB} = V_{THER} – 0.1V	5.4	6.0	6.6	V
Zero duty cycle output voltage	V_{ZERO}		0.9	1.0	1.1	V
Tans-conductance[*1]	G_M		90	115	140	μmho
Maximum Slope Time						
Maximum slope time voltage	VM_{SLP}	R_{SLP} = 40.5KΩ	2.784	2.900	3.016	V
Maximum slope time	T_{OT}	R_{SLP} = 40.5KΩ, T_A=25°C	19	24	29	μS

Current Sense						
Current sense input threshold	V_{CS}		0.7	0.8	0.9	V
Input bias current	I_{BVCS}	V_{CS} = 0 ~ 1 V	–1.0	–0.1	1.0	μA
Current sense delay time[*1]	$T_{VCSDELAY}$	dv/dt = 1V/100nS, from 0V to 5V	–	350	500	nS
Zero Current Detection						
Input voltage threshold[*1]	V_{THZ}		1.35	1.50	1.65	V
Detect Hysteresis[*1]	HY_{ZERO}		0.05	0.10	0.15	V
Input clamp high voltage	V_{CLMPH}	I_{DET} = 3mA	6.0	6.7	7.4	V
Input clamp low voltage	V_{CLMPL}	I_{DET} = –3mA	0	0.65	1.00	V
Input bias current	I_{BZERR}	V_{ZERO} = 1 ~ 5 V	–1.0	–0.1	1.0	μA
Source current[*1]	$I_{SRCZERO}$	T_A=25°C	–	–	–10	mA
Sink current[*1]	$I_{SNKZERO}$	T_A=25°C	–	–	10	mA
Delay time from zero to output[*1]	T_{Z2O}	dv/dt = 1V/100nS, from 5V to 0V	0	–	200	nS
Gate Output						
Gate output high voltage	V_{GOH}	I_O = –100mA, T_A=25°C	9.2	11.0	12.8	V
Gate output low voltage	V_{GOL}	I_O = 200mA, T_A=25°C	–	1.0	2.5	V
Gate output rise time[*1]	T_{GORISE}	C_L=1nF	–	50	100	nS
Gate output fall time[*1]	T_{GOFALL}	C_L=1nF	–	50	100	nS
Maximum gate output voltage	V_{GOUVLO}	V_{DD} = 20V, I_O = 100μA	11.5	13.0	14.5	V
Gate output voltage under UVLO	V_{GOUVLO}	V_{DD} = 5V, I_O = 100μA	–	–	1	V
Restart						
Restart delay time	$T_{DELAYRST}$		50	150	300	μS
Over Voltage Protection						
OVP threshold voltage	V_{OVP}	T_A=25°C	2.620	2.675	2.730	V
OVP Hysteresis	HY_{OVP}	T_A=25°C	0.120	0.175	0.230	V
Enable Function						
Enable threshold voltage	V_{ENB}		0.40	0.45	0.50	V
Enable Hysteresis	HY_{ENB}		0.05	0.10	0.15	V

Notes:
1. Guaranteed by design, not tested in production

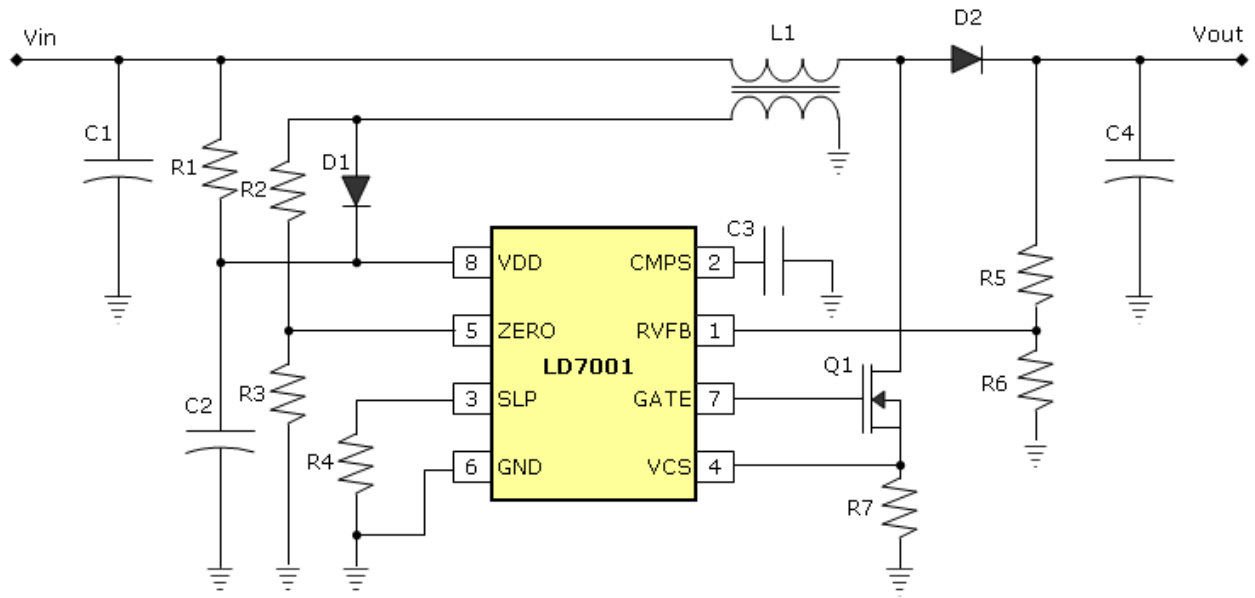
Pin Description

Pin #	Name	Description
1	RVFB	This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V
2	CMPS	This pin is the output of the trans-conductance error amplifier. Components for output voltage compensation should be connected between this pin and GND.
3	SLP	This pin set the slope of the internal ramp. The voltage of this pin is maintained at 2.9V. If a resistor is connected between this pin and GND, current flows out of the pin and the slope of the internal ramp are proportional to this current.
4	VCS	This pin is the input of the over-current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise.
5	ZERO	This pin is the input of the zero current detection block. If the voltage of this pin goes higher than 1.5V, then goes lower than 1.4V, the MOSFET is turned on.
6	GND	This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
7	GATE	This pin is the gate drive output. The peak sourcing and sinking current levels are +500mA and -800mA respectively. For proper operation, the stray inductance in the gate driving path must be minimized.
8	VDD	This pin is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.

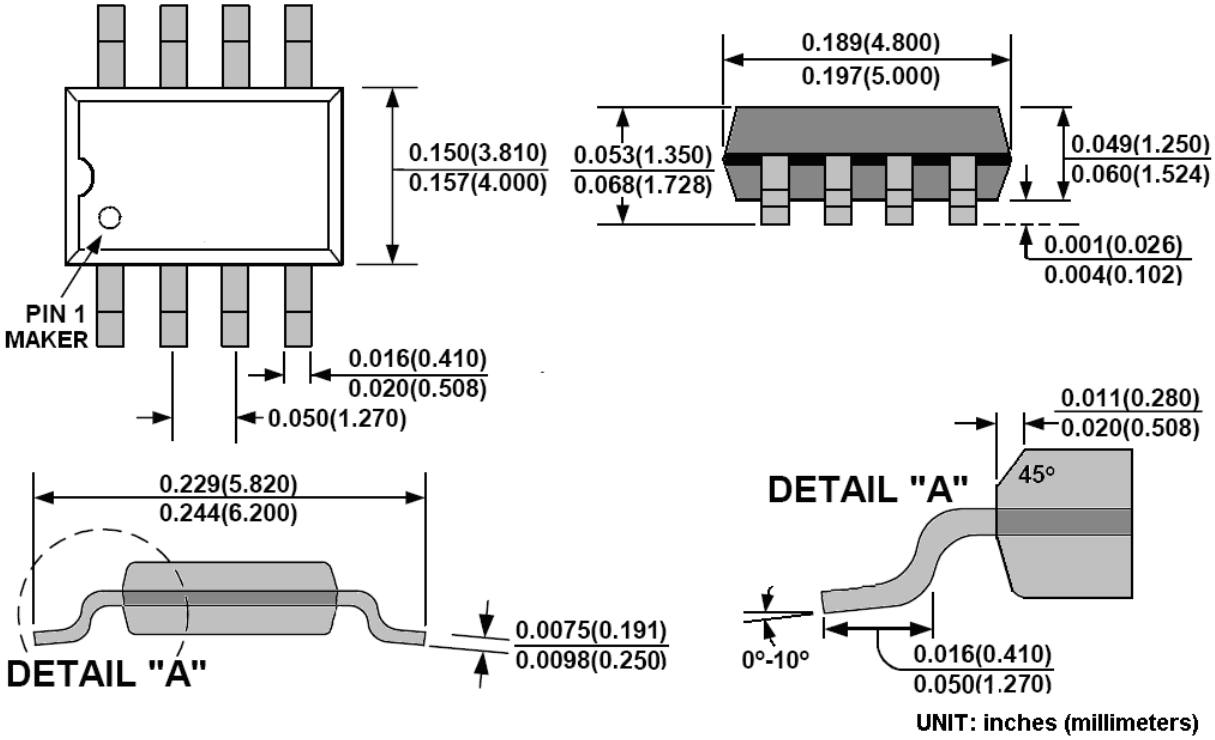
Functional Block Diagram

TBD

Typical Application Circuit



Package Outline



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