亮芯科技股份有限公司
Lighting Device Tech.

Preliminary – **LD6725**

280KHz, 1.5A Boost Regulator

Features

- Integrated Power Switch: 1.5 A Guaranteed
- Wide Input Range: 2.7 V to 30 V
- High Frequency Allows for Small Components
- Minimum External Components
- Easy External Synchronization
- Built in Overcurrent Protection
- Frequency Foldback Reduces Component
- Stress During an Overcurrent Condition
- Thermal Shutdown with Hysteresis
- Shut Down Current: 50 μA Maximum
- Wide Ambient Temperature Range
- Commercial Grade: 0°C to 70°C

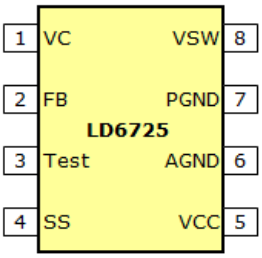
Applications

- Boost regulator

General Description

The LD6725 product is 280 kHz switching regulator with a high efficiency, 1.5 A integrated switch. This part operate over a wide input voltage range, from 2.7V to 30V. The flexibility of the design allows the chip to operate in most power supply configurations, including boost, flyback, forward, inverting, and SEPIC. The ICs utilize current mode architecture, which allows excellent load and line regulation, as well as a practical means for limiting current. Combining high frequency operation with a highly integrated regulator circuit results in an extremely compact power supply solution. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback control.

Package Pin Out

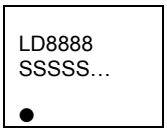


Ordering Information

		Packing Options	
Part No.	Package	Tube (TU)	Tape & Reel (TR)
LD6725	SOP-8	LD6725S1-TU	LD6725S1-TR

- Package material default is “Green” package.

Product Marking



- Line 1 – “LD” is a fixed character
  8888: product name
- Line 2 – SSSSS…: lot number

Absolute Maximum Ratings

Parameter	V_{MIN} ~ V_{MAX}	I_{SOURCE}/I_{SINK}
VCC IC power input	-0.3 ~ +30V	N/A /200mA
SS Shutdown/Sync	-0.3 ~ +30V	1.0mA /1.0mA
VC Loop compensation	-0.3 ~ +6.0V	10mA /10mA
FB Feedback input	-0.3 ~ +10V	1.0mA /1.0mA
Test pin	-0.3 ~ +6.0V	1.0mA /1.0mA
PGND power ground	-0.3 ~ +0.3V	4.0A /10mA
AGND analog ground	0V	N/A /10mA
VSW switch input	-0.3 ~ +40V	10mA /3.0A
Parameter	**Maximum**	**Unit**
T_J Junction temperature range	-40 to +150	°C
T_{STG} Storage temperature range	-65 to +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics

V_{IN} = 12V, V_{COMP} = 0.8V, V_{BST} = V_{IN} + 5V, EN = tied to VIN, SW = open, -40°C≦T_A≦+85°C unless specified

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Error Amplifier						
FB Reference Voltage	V_{REF}	V_C tied to FB; measure at FB	1.246	1.276	1.300	V
FB Input Current	I_{FB}	FB = V_{REF}	-1.0	0.1	1.0	µA
FB Reference Voltage Line Regulation	R_{LINE}	V_C = FB	–	0.01	0.03	%/V
Error Amp Trans-conductance	σ_{ERR}	I_{VC} = ±25 µA	300	550	800	µMho
Error Amp Gain	G_{ERR}	*1	200	500	–	V/V
V_C Source Current	I_{VCSO}	FB = 1.0 V, V_C = 1.25 V	25	50	90	µA
V_C Sink Current	I_{VCSI}	FB = 1.5 V, V_C = 1.25 V	200	625	1500	µA
V_C High Clamp Voltage	V_{CHC}	FB = 1.0 V, V_C sources 25 µA	1.5	1.7	1.9	V
V_C Low Clamp Voltage	V_{CLC}	FB = 1.5 V, V_C sinks 25 µA	0.25	0.50	0.65	V
V_C Threshold	V_{CTH}	Reduce V_C from 1.5 V until switching stops	0.75	1.05	1.30	V
Oscillator						
Base Operating Frequency	F_{BASE}	FB = 1 V	230	280	310	KHz
Reduced Operating Frequency	F_{RED}	FB = 0 V	30	52	120	KHz
Maximum Duty Cycle	DC_{MAX}		90	94	–	%
FB Frequency Shift Threshold	V_{FBSHT}	Frequency drops to reduced operating frequency	0.36	0.40	0.44	V
Sync/Shutdown						
Sync Range	F_{SYNC}		320	–	500	KHz
Sync Pulse Transition Threshold	V_{SYCTH}	Rise time = 20 ns	2.5	–	–	V
SS Bias Current	ISS	SS = 0 V	-15	-3.0	–	µA
		SS = 3.0 V	–	3.0	8.0	
Shutdown Threshold	V_{SDTH}		0.50	0.85	1.20	V
Shutdown Delay	T_{SHDLY}	2.7 V ≤ V_{CC} ≤ 12 V	12	80	350	µs
		12 V < V_{CC} ≤ 30 V	12	36	200	
Power Switch						
Switch Saturation Voltage	V_{SWSAT}	I_{SWITCH} = 1.5 A*1	–	0.8	1.4	V
		I_{SWITCH} =1.0 A, 0°C ≤ T_A≤ 85°C	–	0.55	1.00	
		I_{SWITCH} =1.0 A, -40°C ≤ T_A≤ 0°C*1	–	0.75	1.30	
		I_{SWITCH} = 10 mA	–	0.09	0.45	
Switch Current Limit	I_{SWLMT}	50% duty cycle*1	1.6	1.9	2.4	A
		80% duty cycle*1	1.5	1.7	2.2	

Electrical Characteristics (Cont')

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Minimum Pulse Width	T_{BW}	FB = 0 V, I_{SW} = 4.0 A[*1]	200	250	300	nS
$\Delta I_{CC}/\Delta IV_{SW}$	Ratio	2.7V≤ V_{CC}≤ 12V, 10mA≤ I_{SW}≤ 1.0A	–	10	30	mA/A
		12V≤ V_{CC}≤ 30V, 10mA≤ I_{SW}≤ 1.0A	–	–	100	
		2.7V≤ V_{CC}≤ 12V, 10mA≤ I_{SW}≤ 1.5A[*1]	–	17	30	
		12V≤ V_{CC}≤ 30V, 10mA≤ I_{SW}≤ 1.5A[*1]	–	–	100	
Switch Leakage	I_{SWLK}	V_{SW} = 40 V, V_{CC} = 0V	–	2.0	100	µA
General						
Operating Current	I_{OP}	I_{SW} = 0	–	5.5	8.0	mA
Shutdown Mode Current	I_{SHDN}	V_C< 0.8V, SS=0V, 2.7V≤ V_{CC}≤ 12V	–	12	60	µA
		V_C< 0.8V, SS=0V, 12V≤ V_{CC}≤ 30V	–	–	100	
Minimum Operating Input Voltage	V_{INMIN}	V_{SW} switching, maximum I_{SW} = 10mA	–	2.45	2.70	V
Thermal Shutdown	T_{SHDN}	*1	150	180	210	°C
Thermal Hysteresis	T_{HYST}	*1	–	25	–	°C

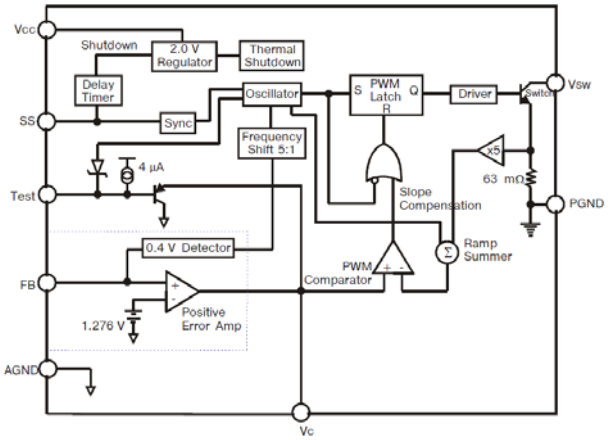
Notes:

1. Guaranteed by design, not 100% tested in production.

Pin Definition

Pin#	Pin Name	Pin Description
1	VC	Loop compensation pin. The VC pin is the output of the error amplifier and is used for loop compensation and current limit. Loop compensation can be implemented by a simple RC network as shown in the application diagram on page 1 as R1 and C1.
2	FB	Positive regulator feedback pin. This pin senses a positive output voltage and is referenced to 1.276 V. When the voltage at this pin falls below 0.4 V, chip switching frequency reduces to 20% of the nominal frequency.
3	Test	This pin is connected to internal test logic and should either be left floating or be used in soft start circuit. Connection to a voltage between 9.5 V and 15 V shuts down the internal oscillator and leaves the power switch running.
4	SS	Synchronization and shutdown pin. This pin may be used to synchronize the part to nearly twice the base frequency. A TTL low will shut the part down and put it into low current mode. If synchronization is not used, this pin should be either tied high or left floating for normal operation..
5	VCC	Input power supply pin. This pin supplies power to the part and should have a bypass capacitor connected to AGND.
6	AGND	Analog ground. This pin provides a clean ground for the controller circuitry and should not be in the path of large currents. The output voltage sensing resistors should be connected to this ground pin. This pin is connected to the IC substrate.
7	PGND	Power ground. This pin is the ground connection for the emitter of the power switching transistor. Connection to a good ground plane is essential.
8	VSW	High current switch pin. This pin connects internally to the collector of the power switch. The open voltage across the power switch can be as high as 40 V. To minimize radiation, use a trace as short as practical.

Block Diagram



Application Information

THEORY OF OPERATION

Current Mode Control

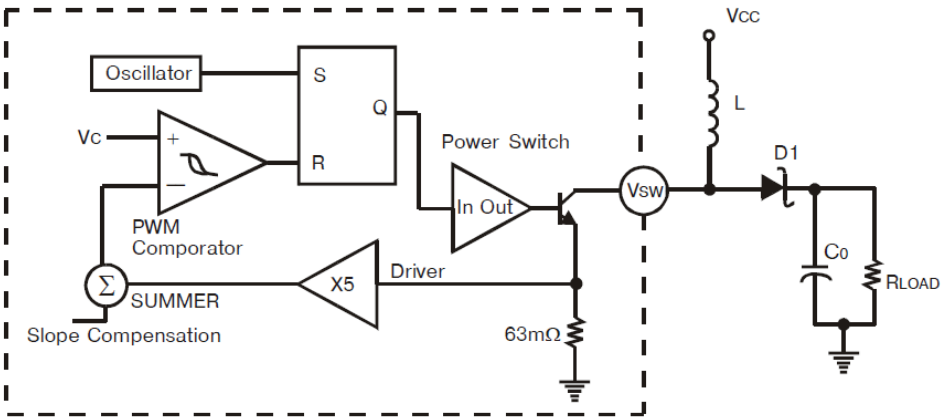


Figure 1. Current Mode Control Scheme

The LD6725 is a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on–time of the power switch. The oscillator is used as a fixed–frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in volt- age mode controllers. The second benefit comes from inherent pulse–by–pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain–bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, sub-harmonic oscillation at duty cycles over 50%. The LD6725 solves this problem by adopting a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Oscillator and Shutdown

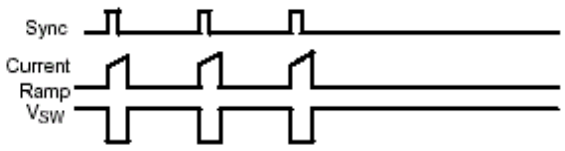


Figure 2. Timing Diagram of Sync and Shutdown

The oscillator is trimmed to guarantee an 18% frequency accuracy. The output of the oscillator turns on the power switch at a frequency of 280 kHz, as shown in Figure
1. The power switch is turned off by the output of the PWM Comparator.

A TTL–compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 2, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby re- setting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.

A sustained logic low at the SS pin will shut down the IC and reduce the supply current.

An additional feature includes frequency shift to 20% of the nominal frequency when the FB pin trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on–time is limited by the PWM comparator minimum pulse width. Extra switch off– time reduces the minimum duty cycle to protect external components and the IC itself.

As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

Error Amplifier

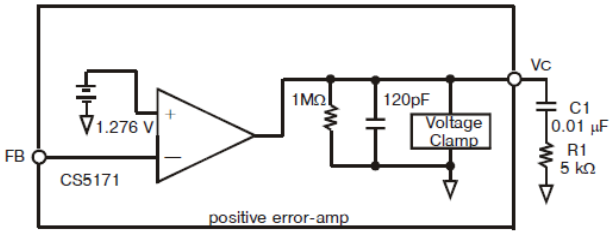


Figure 3. Error Amplifier Equivalent Circuit

The FB pin is directly connected to the inverting input of the positive error amplifier, whose non–inverting input is fed by the 1.276 V reference. The amplifier is trans-conductance amplifier with a high output impedance of approximately 1 MΩ, as shown in Figure 3. The V_C pin is connected to the output of the error amplifiers and is internally clamped between 0.5 V and 1.7 V. A typical connection at the V_C pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the V_C pin and ground to reduce its clamp voltage.

Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

Switch Driver and Power Switch

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (63 mΩ total) to the PGND pin. PGND is not connected to the IC substrate so that switching noise can be isolated from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5A and varies with duty cycle due to slope compensation. The power switch can withstand a maxi- mum voltage of 40 V on the collector (V_{SW} pin). The saturation voltage of the switch is typically less than 1 V to minimize power dissipation.

Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit such as a fuse or relay) has to be implemented to protect the load, power supply and ICs.

In other topologies, the frequency shift built into the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.

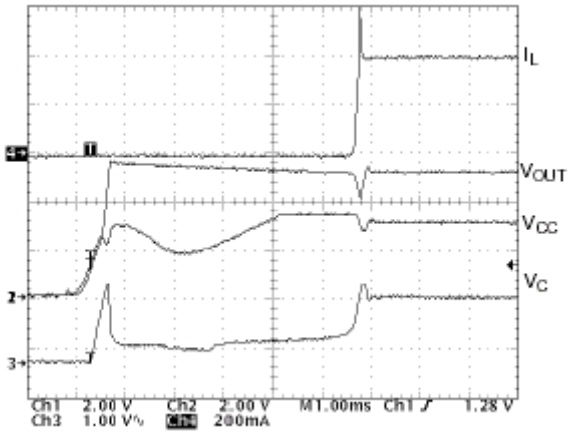


Figure 4. Startup Waveforms of Circuit Shown in the Application Diagram
Load = 400 mA

The LD6725 can be activated by either connecting the V_{CC} pin to a voltage source or by enabling the SS pin. Startup waveforms shown in Figure 4 are measured in the boost converter demonstrated in the Application Diagram on the page 1 of this document. Recorded after the input voltage is turned on, this waveform shows the various phases during the power up transition.

When the V_{CC} voltage is below the minimum supply voltage, the V_{SW} pin is in high impedance. Therefore, current conducts directly from the input power source to the output through the inductor and diode. Once V_{CC} reaches approximately 1.5 V, the internal power switch briefly turns on. This is a part of the LD6725 normal operation. The turn on of the power switch accounts for the initial current swing.

When the V_C pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the V_{SW} pin. Detecting a low output voltage at the FB pin, the built–in frequency shift feature reduces the switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is other- wise limited by the minimum on–time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V, the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull–on, by which the sink current of the error amplifier is increased once an overvoltage condition is de- tected. The overvoltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

COMPONENT SELECTION

Frequency Compensation

The goal of frequency compensation is to achieve desirable transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in Figure 5, provides a frequency response of two poles and one zero. This frequency response is further illustrated in the Bode plot shown in Figure 6.

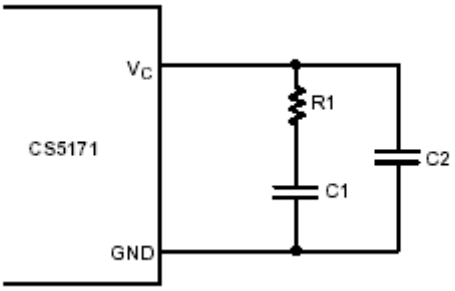


Figure 5. A Typical Compensation Network

The high DC gain in Figure 6 is desirable for achieving DC accuracy over line and load variations. The DC gain of a trans-conductance error amplifier can be calculated as follows:

$$Gain_{DC} = G_M \times R_0$$

where:
G_M = error amplifier trans-conductance;
R_0 =error amplifier output resistance ≈1MΩ.
The low frequency pole, f_{P1}, is determined by the error amplifier output resistance and C1 as:

$$f_{P1} = \frac{1}{2\pi C1 R_0}$$

The first zero generated by C1 and R1 is:

$$f_{Z1} = \frac{1}{2\pi C1 R1}$$

The phase lead provided by this zero ensures that the loop has at least a 45° phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency.

$$f_P = \frac{1}{2\pi C_0 R_{LOAD}}$$

where
C_0 = equivalent output capacitance of the error amplifier
≈ 120pF;
R_{LOAD}= load resistance.

The high frequency pole, f_{P2}, can be placed at the output filter's ESR zero or at half the switching

frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C2 and R1:

$$f_{P2} = \frac{1}{2\pi C2R1}$$

One simple method to ensure adequate phase margin is to design the frequency response with a –20 dB per decade slope, until unity–gain crossover. The crossover frequency should be selected at the midpoint between f_{Z1} and f_{P2} where the phase margin is maximized.

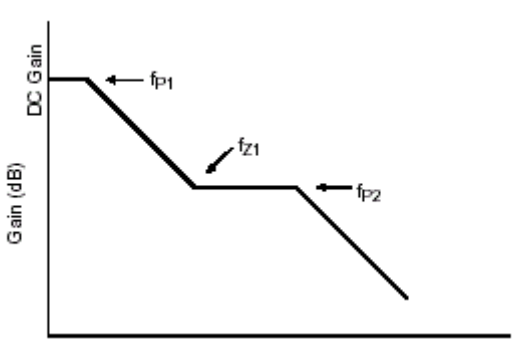


Figure 6. Bode Plot of the Compensation Network Shown in Figure 5

V_{SW} Voltage Limit

In the boost topology, V_{SW} pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5V for Schottky diodes and 0.8V for ultrafast recovery diodes

$$V_{SW(MAX)}=V_{OUT(MAX)}+V_F$$

where:

V_F = output diode forward voltage.

In the flyback topology, peak VSW voltage is governed by:

$$V_{SW(MAX)}=V_{CC(MAX)}+(VOUT+V_F)xN$$

where:

N = transformer turns ratio, primary over secondary.

When the power switch turns off, there exists a voltage spike superimposed on top of the steady–state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the V_{SW} and PGND pins. To prevent the voltage at the V_{SW} pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the V_{SW} pin and ground.

Magnetic Component Selection

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain (V_{OUT}/V_{CC}), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$I_{RIPPLE} = \frac{V_{CC}(V_{OUT} - V_{CC})}{(f)(L)(V_{OUT})}$$

where:

f=280 kHz

The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

Input Capacitor Selection

In boost circuits, the inductor becomes part of the in- put filter, as shown in Figure 8. In continuous mode, the input current waveform is triangular and does not contain a large pulsed current, as shown in Figure 7. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from Figure 7, the product of the inductor current ripple and the input capacitor's effective series resistance (ESR) determine the V_{CC} ripple. In most applications, input capacitors in the range of 10 µF to 100 µF with an ESR less than 0.3 Ω work well up to a full 1.5 A switch current.

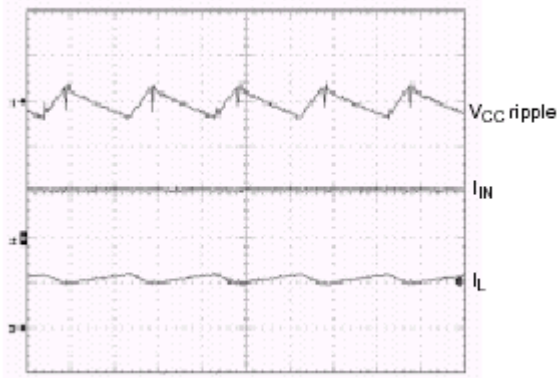


Figure 7. Boost Input Voltage and Current Ripple Waveforms

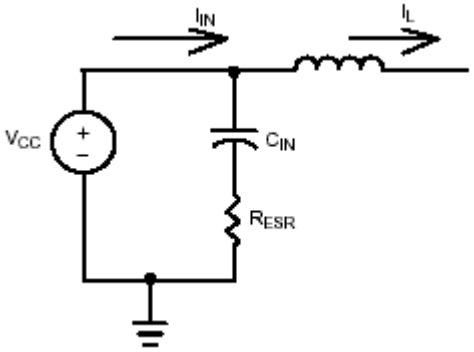


Figure 8. Boost Circuit Effective Input Filter

The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is seen by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator: energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than 20 µF with low ESR is required. To reduce the noise generated by the inductor, insert a 1.0 µF ceramic capacitor between V_{CC} and ground as close as possible to the chip.

By examining the waveforms shown in Figure 9, we can see that the output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, I_L flows into the output capacitor causing an instant $\Delta V = I_{IN} \times ESR$. At the same time, current $I_L - I_{OUT}$ charges the capacitor and increases the output voltage gradually.

Output Capacitor Selection

Figure 9. Typical Output Voltage Ripple

When the power switch is turned on, I_L is shunted to ground and I_{OUT} discharges the output capacitor. When the I_L ripple is small enough, I_L can be treated as a constant and is equal to input current I_{IN}. Summing up, the output voltage peak–peak ripple can be calculated by:

$$V_{OUT(RIPPLE)} = \frac{(I_{IN} - I_{OUT})(1-D)}{(C_{OUT})(f)} + \frac{I_{OUT} D}{(C_{OUT})(f)} + I_{IN} \times ESR$$

The equation can be expressed more conveniently in terms of V_{CC}, V_{OUT} and I_{OUT} for design purposes as follows:

$$V_{OUT(RIPPLE)} = \frac{I_{OUT}(V_{OUT} - V_{CC})}{(C_{OUT})(f)} \times \frac{1}{(C_{OUT})(f)} + \frac{(I_{OUT})(V_{OUT})(ESR)}{V_{CC}}$$

The capacitor RMS ripple current is:

$$I_{RIPPLE} = \sqrt{(I_{IN} - I_{OUT})^2 (1-D) + (I_{OUT})^2 (D)} = I_{OUT} \sqrt{\frac{V_{OUT} - V_{CC}}{V_{CC}}}$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

Reducing the Current Limit

In some applications, the designer may prefer a lower limit on the switch current than 1.5 A. An external shunt can be connected between the V_C pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

The voltage on the V_C pin can be evaluated with the equation

$$V_C = I_{SW} R_E A_V$$

where:

R_E= 0.063Ω , the value of the internal emitter resistor;

A_V=5 V/V, the gain of the current sense amplifier.

Since R_E and A_V cannot be changed by the end user, the only available method for limiting switch current below 1.5 A is to clamp the V_C pin at a lower voltage. If the maxi- mum switch or inductor current is substituted into the equation above, the desired clamp voltage will result.

A simple diode clamp, as shown in Figure 10, clamps the V_C voltage to a diode drop above the voltage on resistor R3. Unfortunately, such a simple circuit is not generally acceptable if V_{IN} is loosely regulated.

Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in Figure 11.

The switch current is limited to

$$I_{SWITCH(PEAK)} = \frac{V_{BE(Q1)}}{R_{SENSE}}$$

where:

$V_{BE(Q1)}$=the base–emitter voltage drop of Q1, typically 0.65V.

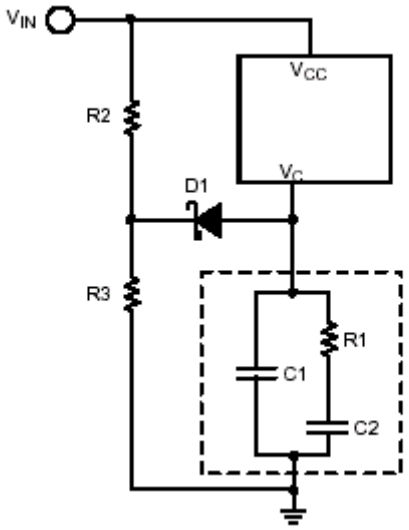


Figure 10. Current Limiting using a Diode Clamp

The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor, RSENSE, results in a considerable power loss which increases with the duty cycle. Resistor R2 and capacitor C3 form a low–pass filter to remove noise.

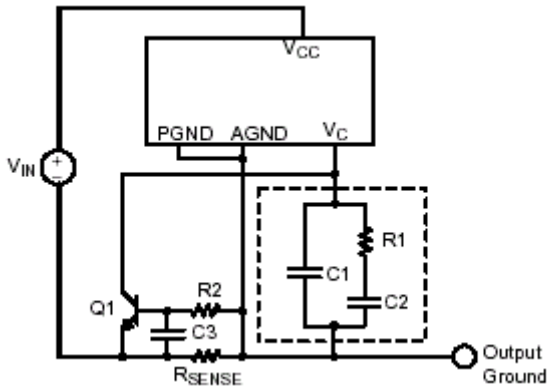


Figure 11. Current Limiting using a Current Sense Resistor

Sub-harmonic Oscillation

Sub-harmonic oscillation (SHM) is a problem found in current mode control systems, where instability results when duty cycle exceeds 50%. SHM only occurs in switching regulators with a continuous inductor current. This in- stability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high frequency audible noise.

SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal “slope compensation” to prevent any duty cycle instability from carrying through to the next switching cycle. In the LD6725, slope compensation is added during the entire switch on-time, typically in the amount of 180 mA/μs.

In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is more slope compensation to avoid the unwanted oscillation. In that case, an external circuit, shown in Figure 40, can be added to increase the amount of slope compensation used. This circuit requires only a few components and is “tacked on” to the compensation network.

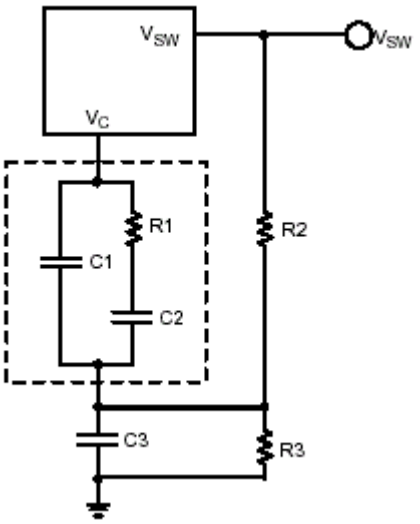


Figure 12. Technique for Increasing Slope Compensation

The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors R2 and R3 form a voltage divider off of the V_{SW} pin. In normal operation, V_{SW} looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating V_{SW} in the boost and flyback topologies are given in the section "V_{SW} Voltage Limit." The voltage on V_{SW} charges capacitor C3 when the switch is off, causing the voltage at the V_C pin to shift upwards. When the switch turns on, C3 discharges through R3, producing a negative slope at the V_C pin. This negative slope provides the slope compensation.

The amount of slope compensation added by this circuit is

$$\frac{\Delta I}{\Delta T} = V_{SW}\left(\frac{R_3}{R_2+R_3}\right)\left(1-e^{\frac{-(1-D)}{R_3C_3f_{SW}}}\right)\left(\frac{f_{SW}}{(1-D)R_E A_V}\right)$$

where:

$\Delta I/\Delta T$ = the amount of slope compensation added (A/s);

V_{SW} = the voltage at the switch node when the transistor is turned off (V);

f_{SW} = the switching frequency, typically 280 kHz;

D = the duty cycle;

R_E = 0.063 Ω , the value of the internal emitter resistor;

A_V = 5 V/V, the gain of the current sense amplifier.

In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, and then select values for R2 and R3 such that the amount of slope compensation added is 100 mA/µs. Then R2 may be increased or decreased as necessary. Of course, the series combination of R2 and R3 should be large enough to avoid drawing excessive current from VSW. Additionally, to ensure that the control loop stability is improved, the time constant formed by the additional components should be chosen such that

$$R_3C_3 \langle \frac{1-D}{f_{SW}}$$

Finally, it is worth mentioning that the added slope compensation is a trade–off between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

Soft Start

Through the addition of an external circuit, a soft–start function can be added to the LD6725. Soft–start circuitry prevents the V_C pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope.

This circuit, shown in Figure 13, requires a minimum number of components and allows the soft–start circuitry to activate any time the SS pin is used to restart the converter.

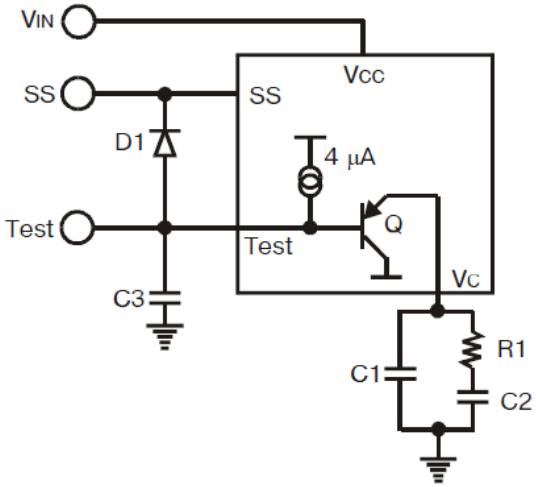


Figure 13. Soft Start

Resistor R1 and capacitors C1 and C2 form the compensation network. At turn on, the voltage at the V_C pin starts to come up, charging capacitor C3 through transistor Q, clamping the voltage at the V_C pin such that switching begins when V_C reaches the V_C threshold, typically 1.05 V.

Therefore, C3 slows the startup of the circuit by limiting the voltage on the V_C pin. The soft–start time increases with the size of C3.

Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to V_{IN}.

Calculating Junction Temperature

To ensure safe operation of the LD6725, the designer must calculate the on–chip power dissipation and determine its expected junction temperature. Internal thermal protection circuitry will turn the part off once the junction temperature exceeds 180°C±30°. However, repeated operation at such high temperatures will ensure a reduced operating life.

Calculation of the junction temperature is an imprecise but simple task. First, the power losses must be quantified. There are three major sources of power loss on the LD6725:

- biasing of internal control circuitry, P_{BIAS}
- switch driver, P_{DRIVER}
- switch saturation, P_{SAT}

The internal control circuitry, including the oscillator and linear regulator, requires a small amount of power even when the switch is turned off. The specifications section of this datasheet reveals that the typical operating current, I_Q, due to this circuitry is 5.5mA. Additional guidance can be found in the graph of operating current vs. temperature. This graph shows that I_Q is strongly dependent on input voltage, V_{IN}, and the ambient temperature, T_A. Then

$$P_{BIAS}=V_{IN}I_Q$$

Since the onboard switch is an NPN transistor, the base drive current must be factored in as well. This current is drawn from the V_{IN} pin, in addition to the control circuitry current. The base drive current is listed in the specifications as $\Delta I_{CC}/\Delta I_{SW}$, or switch trans-conductance. As before, the designer will find additional guidance in the graphs. With that information, the designer can calculate

$$P_{DRIVER} = V_{IN} I_{SW} \times \frac{I_{CC}}{\Delta I_{SW}} \times D$$

where:
I_{SW}=the current through the switch;
D=the duty cycle or percentage of switch on–time.

I_{SW} and D are dependent on the type of converter. In a boost converter,

$$I_{SW(AVG)} \cong I_{LOAD} \times D \times \frac{1}{Efficiency}$$

$$D \cong \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

In a Flyback converter,

$$I_{SW(AVG)} \cong \frac{V_{OUT} I_{LOAD}}{V_{IN}} \times \frac{1}{Efficiency}$$

$$D \cong \frac{V_{OUT}}{V_{OUT} + \frac{N_S}{N_P} V_{IN}}$$

The switch saturation voltage, $V_{(CE)SAT}$, is the last major source of on–chip power loss. $V_{(CE)SAT}$ is the collector– emitter voltage of the internal NPN transistor when it is driven into saturation by its base drive current. The value for $V_{(CE)SAT}$ can be obtained from the specifications or from the graphs, as “Switch Saturation Voltage.” Thus,

$$P_{SAT} \cong V_{(CE)SAT} I_{SW} \times D$$

Finally, the total on–chip power losses are

$$P_D = P_{BIAS} + P_{DRIVER} + P_{SAT}$$

Power dissipation in a semiconductor device results in the generation of heat in the junctions at the surface of the chip. This heat is transferred to the surface of the IC pack- age, but a thermal gradient exists due to the resistive proper- ties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturers’ data sheets as Θ_{JA}, or junction–to–ambient thermal resistance. The on–chip junction temperature can be calculated if Θ_{JA}, the air temperature near the surface of the IC, and the on-chip power dissipation are known.

$$T_J = T_A + (P_D \Theta_{JA})$$

where:
T_J = IC or FET junction temperature (°C);
T_A = ambient temperature (°C);
P_D = power dissipated by part in question (W);
Θ_{JA} = junction–to–ambient thermal resistance (°C/W). For the LD6725 Θ_{JA}=165°C/W.

Once the designer has calculated T_J, the question whether the LD6725 can be used in an application is settled. If T_J exceeds 150°C, the absolute maximum allowable junction temperature, the LD6725 is not suitable for that application.

If T_J approaches 150°C, the designer should consider possible means of reducing the junction temperature. Perhaps another converter topology could be selected reduce the switch current. Increasing the airflow across the surface of the chip might be considered to reduce T_A.

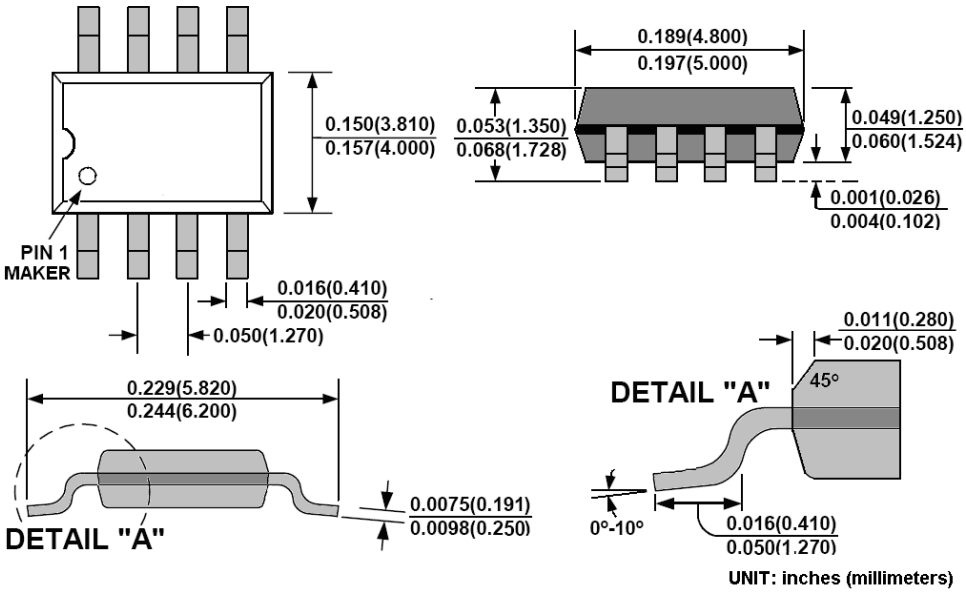
Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on–chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on–chip power transistor, while the trans- former, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best result.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.

Package Outline

SOP8:



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