Features

- Operation from 3.0 V to 40 V input
- Low standby current
- Current limiting
- Output switch current up to 1.5 A
- Adjustable output voltage
- Operation at frequencies up to 100KHz
- Precision reference (2%)

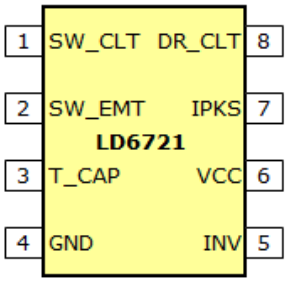
Applications

- Battery Chargers
- NICs/Switches/Hubs
- ADSL Modems
- Negative Voltage Power Supplies

General Description

The LD6721 series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature-compensated reference, comparator, and controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in step-down and step-up and voltage-inverting applications with a minimum number of external components.

Package Pin Out

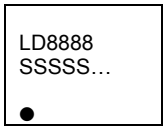


Ordering Information

		Packing Options	
Part No.	Package	Tube (TU)	Tape & Reel (TR)
LD6721	SOP-8	LD6721S1-TU	LD6721S1-TR

- Package material default is “Green” package.

Product Marking



- Line 1 – “LD” is a fixed character
  8888: product name
- Line 2 – SSSSS…: lot number

Pin Definition

Pin#	Pin	Pin Name	Pin Description
1	SW_CLT	Switch Collector	Internal switch transistor collector
2	SW_EMT	Switch Emitter	Internal switch transistor emitter
3	T_CAP	Timing Capacitor	Timing Capacitor to control the switching frequency
4	GND	GND	Ground pin for all internal circuits
5	INV	Inverting Input	Inverting input pin for internal comparator
6	VCC	VCC	Voltage supply
7	IPKS	IPK Sense	Peak Current Sense Input by monitoring the voltage drop across an external I sense resistor to limit the peak current through the switch
8	DR_CLT	Driver Collector	Voltage driver collector

Absolute Maximum Ratings

Parameter	Maximum	Unit
V_{CC} power supply voltage	40	V
V_{IR} comparator input voltage	-0.3 to +40	V
$V_{C(SW)}$, $V_{E(SW)}$, $V_{CE(SW)}$, and $V_{C(DR)}$ voltage	40	V
Driver collector current *1	100	mA
I_{SW} switch current	1.5	A
Operating junction temperature	150	°C
Operating ambient temperature range	-40 to +85	°C
Storage temperature range	-65 to +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics *1

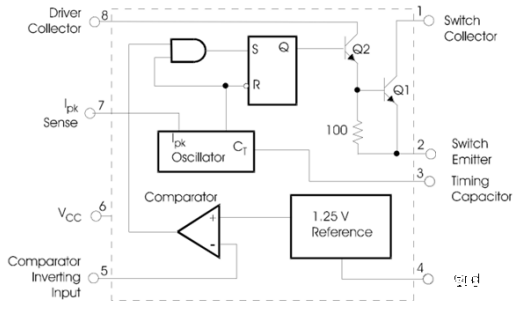
V_{CC}=5.0V, -40°C≦T_A≦+85°C unless specified

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillator						
Frequency	F_{OSC}	V_{Pin5}=0V, C_T=1.0nF, T_A=25°C	24	33	42	kHz
Charge current	I_{CHG}	V_{CC}=5.0V to 40V, T_A=25°C	24	35	42	μA
Discharge current	I_{DISCHG}	V_{CC}=5.0V to 40V, T_A=25°C	140	220	260	μA
Discharge-to-charge current ratio	Ratio	I_{DISCHG}/I_{CHG}, Pin7 to V_{CC}, T_A=25°C	5.2	6.5	7.5	–
Current limit sense voltage	V_{PKSLMT}	$I_{CHG}=I_{DISCHG}$, T_A=25°C	250	300	350	mV
Output Switch *2						
Saturation voltage, Darlington connection	V_{CESAT}	I_{Sw}=1.0A, Pins1, 8 connected	–	1.0	1.3	V
		I_{Sw}=1.0A, R_{Pin8}=82Ω to V_{CC}, forced β =20	–	0.45	0.7	
DC current gain	hfe	I_{Sw}=1.0A, V_{CE}=5.0, T_A=25°C	50	75	–	–
Collector off-state current	$I_{C(OFF)}$	V_{CE}=40V	–	40	100	μA
Comparator						
Threshold voltage	V_{TH}	–	1.225	1.25	1.275	V
		*3	1.21	–	1.29	
Threshold voltage line regulation	R_{LINE}	V_{CC}=3.0V to 40V	–	1.4	5.0	mV
Input bias current	I_{IB}	V_{in}=0V	–	-20	-400	nA
Total Device						
Supply current	I_{CC}	V_{CC}=5.0V to 40V, C_T=1.0nF, V_{Pin7} =V_{CC}, V_{Pin5}>V_{TH}, V_{Pin2} =GND, other pins - open	–	–	4.0	mA

Notes:

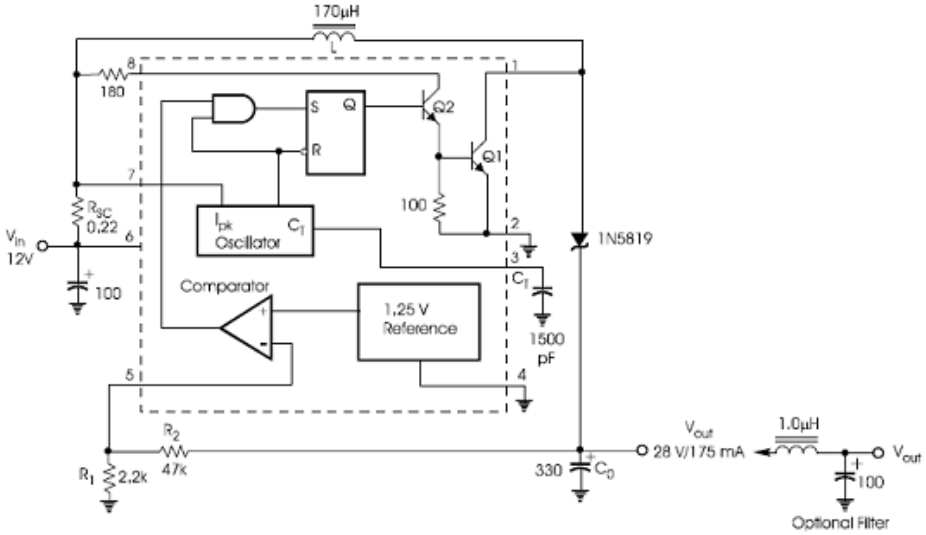
1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during the test to maintain junction temperature as close to ambient temperature as possible.
3. This applied over full operation temperature range.

Block Diagram



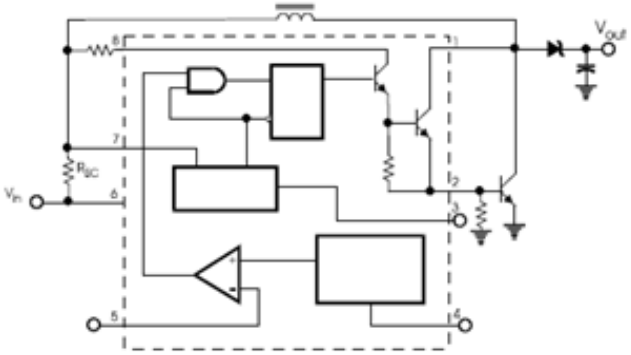
Typical Application Circuit

1. Step–up converter

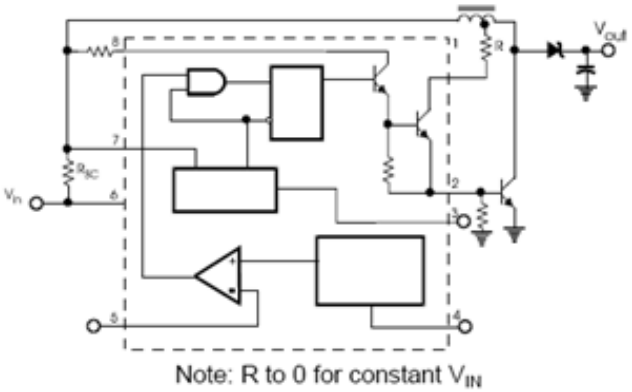


2. External current boost connections for IC Peak greater than 1.5A

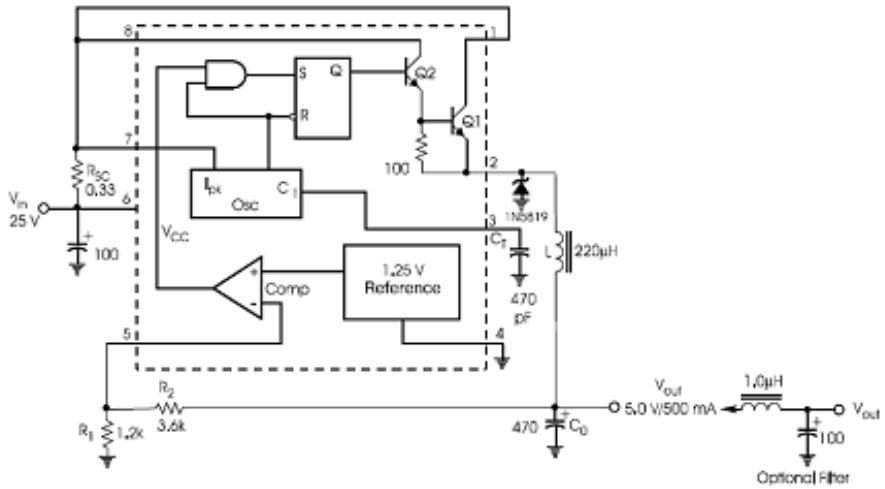
A. External NPN switch



B. External NPN saturated switch

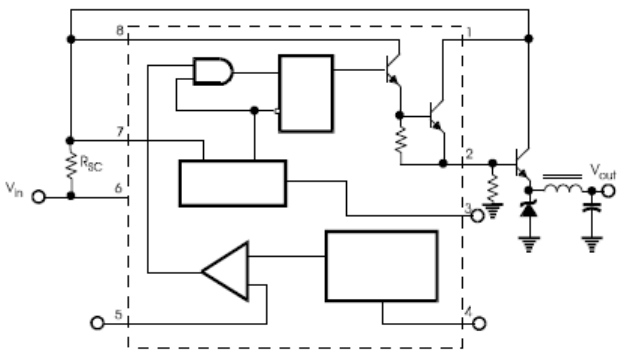


3. Step-down converter

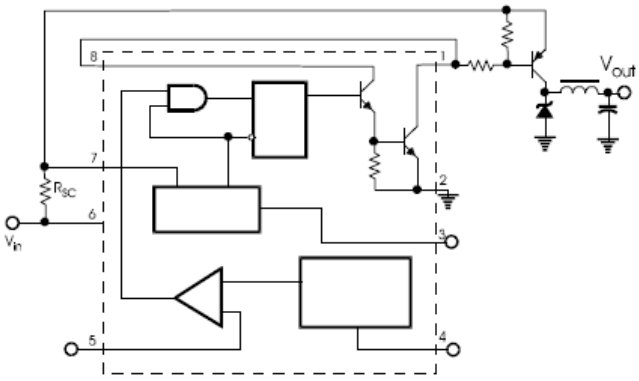


4. External current boost connections for IC Peak greater than 1.5A

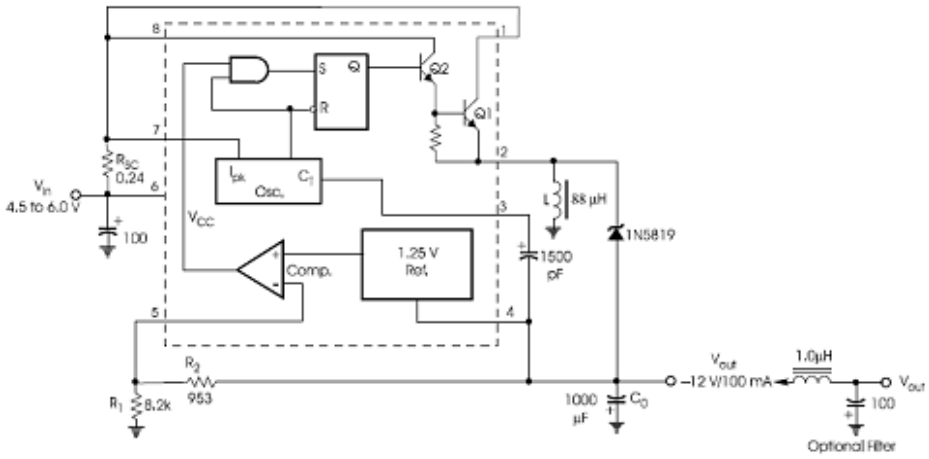
A. External NPN switch



B. External NPN saturated switch



5. Voltage inverting converter



DESIGN FORMULA

Calculation	Step-up	Step-down	Voltage-inverting
t_{on}	$\frac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$	$\frac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$	$\frac{\lvert V_{out}\rvert+V_F}{V_{in}+V_{sat}}$
$(t_{on}+t_{off})max$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0\times10^{-5}\,t_{on}$	$4.0\times10^{-5}\,t_{on}$	$4.0\times10^{-5}\,t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}}+1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}}+1\right)$
R_{sc}	$0.3/I_{pk(Switch)}$	$0.3/I_{pk(Switch)}$	$0.3/I_{pk(Switch)}$
$L_{(min)}$	$\left(\frac{V_{in(min)}-V_{sat}}{I_{pk(switch)}}\right)\times t_{on(max)}$	$\left(\frac{V_{in(min)}-V_{sat}-V_{out}}{I_{pk(switch)}}\right)\times t_{on(max)}$	$\left(\frac{V_{in(min)}-V_{sat}}{I_{pk(switch)}}\right)\times t_{on(max)}$
C_o	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on}+t_{off})}{8V_{ripple(pp)}}$	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$

TERMS AND DEFINITIONS

V_{sat} – Saturation voltage of the output switch.

V_f – Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.

Vout – Desired output voltage, $|V_{out}|=1.25\left(1+\frac{R_2}{R_1}\right)$

f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_{out}.

$V_{ripple(p-p)}$ – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

Typical Performance Characteristics

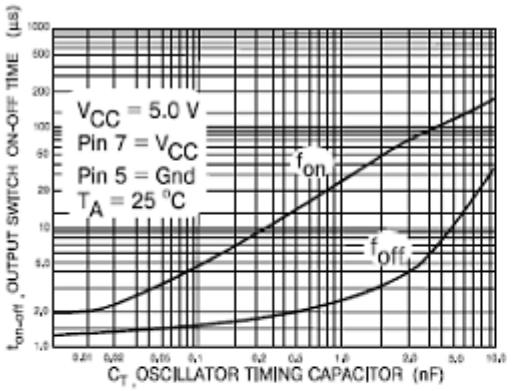


Fig.1. Output Switch on-off time versus Oscillator timing capacitor

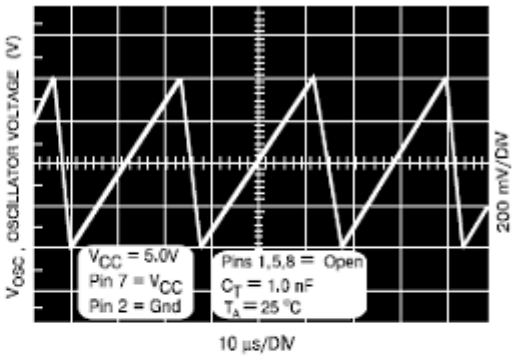


Fig.2. Timing capacitor waveform

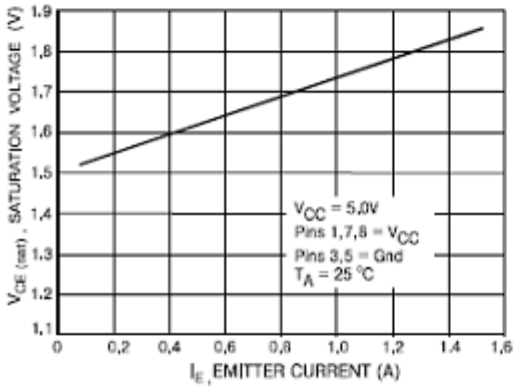


Fig.3. Emitter follower configuration output saturation voltage versus Emitter current

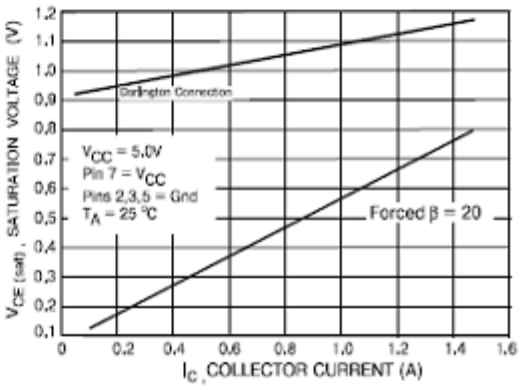


Fig.4. Common emitter configuration output saturation voltage versus Collector current

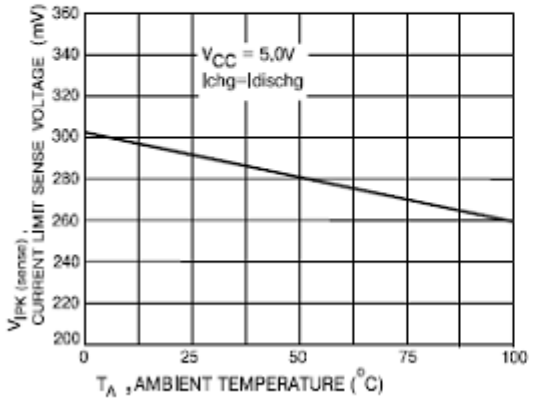


Fig.5. Current limit sense voltage versus Temperature

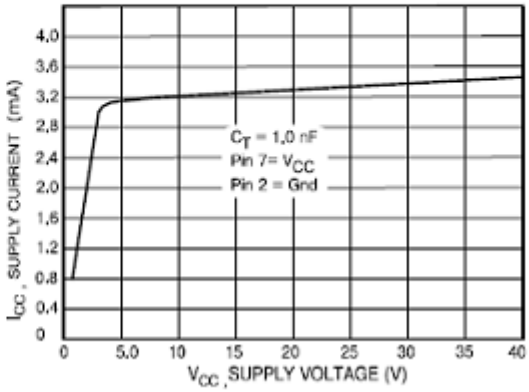
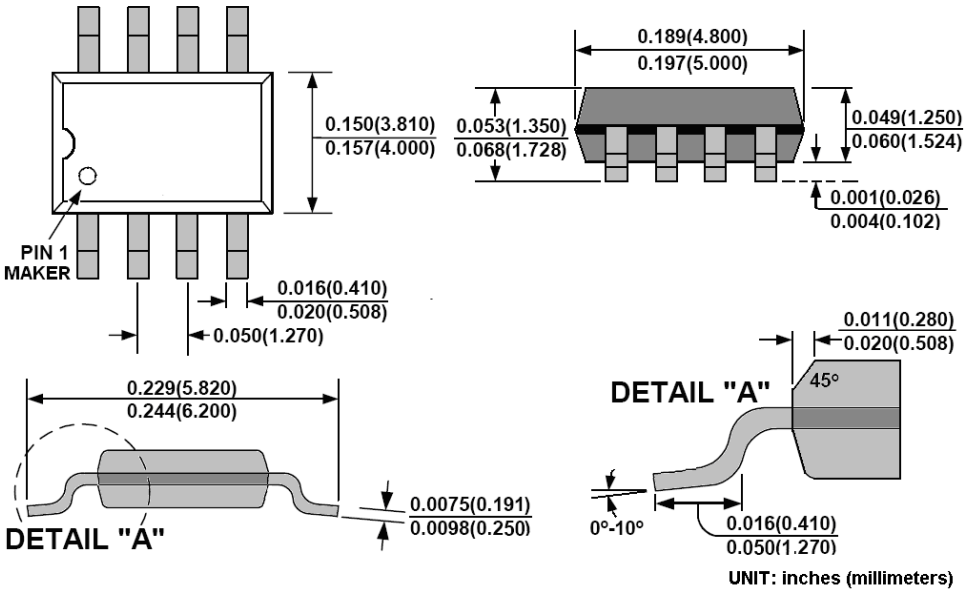


Fig.6. Standby supply current versus Supply voltage

Package Outline

SOP8:



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