Preliminary – **LD6326**

150mA Low Noise
LDO Regulator

Features

- Ultralow-noise output
- High output voltage accuracy
- Guaranteed 150mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse-battery protection
- “Zero” off-mode current
- Logic-controlled electronic enable

Applications

- Cellular telephones
- Laptop, notebook, and palmtop computers
- Battery-powered equipment
- PCMCIA VCC and VPP regulation/switching
- Consumer/personal electronics
- SMPS post-regulator/dc-to-dc modules
- High-efficiency linear power supplies

General Description

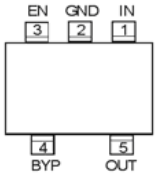
The LD6326 is an efficient linear voltage regulator with an ultralow-noise output, a very low dropout voltage (typically 17mV at light loads and 165mV at 150mA), and a very low ground current (600 A at 100mA output). The LD6326 offers better than 1% initial accuracy.

Designed especially for hand-held, battery-powered devices, the LD6326 includes a CMOS- or TTL-compatible enable/shutdown control input. When shut down, its power consumption drops nearly to zero. The regulator ground current increases only slightly in a dropout, further prolonging the battery life.

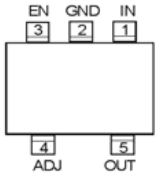
The LD6326 key features are a reference bypass (BYP) pin to improve its already excellent low- noise performance, reversed-battery protection, current limiting, and over temperature shutdown. The LD6326 is available in fixed (-XX) and adjustable (Adj) output voltage versions in a small SOT-23-5 package.

The fixed output voltage version LD6326 may have a nominal output voltage (XX) within 1.5V to 12V.

Package Pin Out



Fixed Voltages



Adjustable Voltage

Ordering Information

		Packing Options	
Part No.	Package	Tube (TU)	Tape & Reel (TR)
LD6326	SOT23-5	LD6326L2-TU	LD6326L2-TR

- Package material default is “Green” package.

Product Marking

LD8888 SSSSS… ●

- ✧ Line 1 – “LD” is a fixed character
  8888: product name
- ✧ Line 2 – SSSSS…: lot number

Absolute Maximum Ratings[*1]

Parameter	Maximum	Unit
Supply input voltage (VIN)	-20 to +20	V
EN (enable) input voltage (VEN)	-20 to +20	V
Power dissipation (PD)	Internally limited[*2]	
Lead temperature (soldering, 5 sec.)	260	°C
Junction temperature (TJ)	-40 to +125	°C
Storage temperature (TSTG)	-65 to +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

OPERATING RATINGS[*3]

Parameter	Maximum	Unit	Parameter	Maximum	Unit
Input voltage (VIN)	-2 to +16	V	Junction temperature (TJ)	-40 to +125	°C
EN input voltage (VEN)	0 to +VIN	V	Thermal resistance, SOT-23-5 (JA)	*2	°C

Electrical Characteristics

$V_{IN}=V_{OUT}+1V$, $I_L=100$ A, $C_L=1.0$ F, $V_{EN}=2.0V$, TJ=25°C, unless specified otherwise; the **bold** values indicate -40°C≦TJ≦+125°C

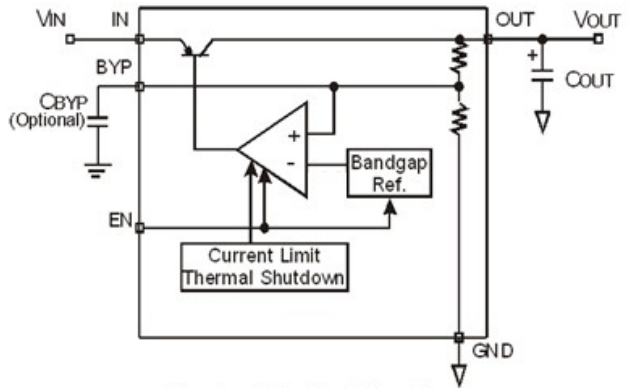
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Voltage Accuracy	V_O[*4]	Variation from specified V_{OUT}, TJ = 25°C	-1	–	1	%
		Variation from specified V_{OUT}, -40°C≦TJ≦+125°C	**-2**	–	**2**	
Output Voltage Temp. Coefficient	$\Delta V_O/\Delta T$	*5	–	40	–	ppm/°C
Line Regulation	$\Delta V_O/V_O/V_I$	$V_{IN}=V_{OUT}+1V$ to 16V, TJ = 25°C	–	0.004	0.012	%
		$V_{IN}=V_{OUT}+1V$ to 16V, -40°C≦TJ≦+125°C			**0.05**	
Load Regulation[*6]	$\Delta V_O/V_O$	I_L=0.1mA to 150 mA, TJ = 25°C	–	0.02	0.2	%
		I_L=0.1mA to 150 mA, -40°C≦TJ≦+125°C			**0.5**	
Dropout Voltage[*7]	V_{IN}-V_{OUT}	I_L=100μA	–	10	50	mV
		I_L=50mA	–	110	150	
		I_L=100mA	–	140	250	
		I_L=150mA	–	165	275	
Quiescent Current	I_Q	V_{EN} ≤ 0.4V (shutdown)	–	0.01	1	μA
		V_{EN} ≤ 0.18V (shutdown)	–	–	5	
Ground Pin Current[*8]	I_{GND}	I_L=100μA, V_{EN} ≥ 2.0V, (active)	–	120	160	μA
		I_L=50mA, V_{EN} ≥ 2.0V, (active)	–	350	600	
		I_L=100mA, V_{EN} ≥ 2.0V, (active)	–	600	800	
		I_L=150mA, V_{EN} ≥ 2.0V, (active)	–	1300	1900	
Current Limit	I_{LIMIT}	V_{OUT}=0 V	–	320	600	mA
Enable Input						
Enable Input Logic Low Voltage	V_{IL}	Regulator shut-down, TJ = 25°C	–	–	0.4	V
		Regulator shut-down, -40°C≦TJ≦+125°C	–	–	**0.18**	V
EN input logic High voltage	V_{IH}	Regulator enabled	2.0	–	–	V
Enable Input Current	I_{IL}	V_{IL} ≤ 0.4 V	–	0.01	1	μA
		V_{IL} ≤ 0.18 V	–	–	2	μA
Enable Input Current	I_{IH}	V_{IH} ≥ 2.0 V	2	5	35	μA
		V_{IH} ≥ 2.0 V	–	–	40	μA

Notes: 1. Exceeding the absolute maximum rating may damage the device. 2. The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)}–T_A)+\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The LD6326 (all versions)θ_{JA} value is 220°C/W (the chip is mounted on a PC board). 3. The device is not guaranteed to function outside its operating rating. 4. LD6326A has V_{REF}=1.242±1%, but the minimum output voltage for LD6326A must be above $V_{OUT(min)}$ = 1.5V 5. The **Output voltage temperature coefficient** is defined as the worst case voltage change divided by the total temperature range. 6. The **Load regulation** is measured at a constant junction temperature using low duty cycle pulse testing. The parts per this parameter are tested in the load range of 0.1mA to 150mA. 7. The **Dropout voltage** is defined as the input-to-output differential, at which the output voltage drops 2% below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2 V must be taken into account. 8. The **GND pin current** is the regulator Quiescent current plus the pass transistor base current. The total current drawn from the supply is the sum of the load current plus the GND pin current.

Pin Description

Name	Description
IN	Supply input
GND	Ground
EN	Enable/Shutdown input: CMOS-compatible. Logic High = Enabled. Logic Low or Open = Shut-down.
BYP	Reference bypass: connect external 470pF capacitor to GND to reduce output noise. May be left open.
ADJ	Adjust input: adjustable regulator feedback input. Connect to resistor voltage divider
OUT	Regulator output

Block Diagram



Typical Application Circuits

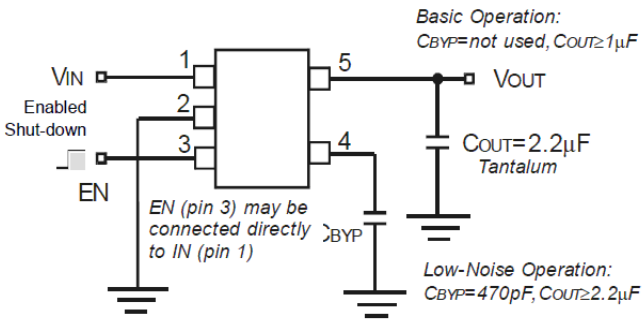


Fig 1. Ultralow noise regulator

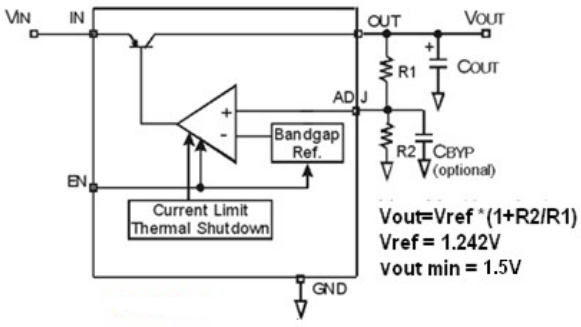
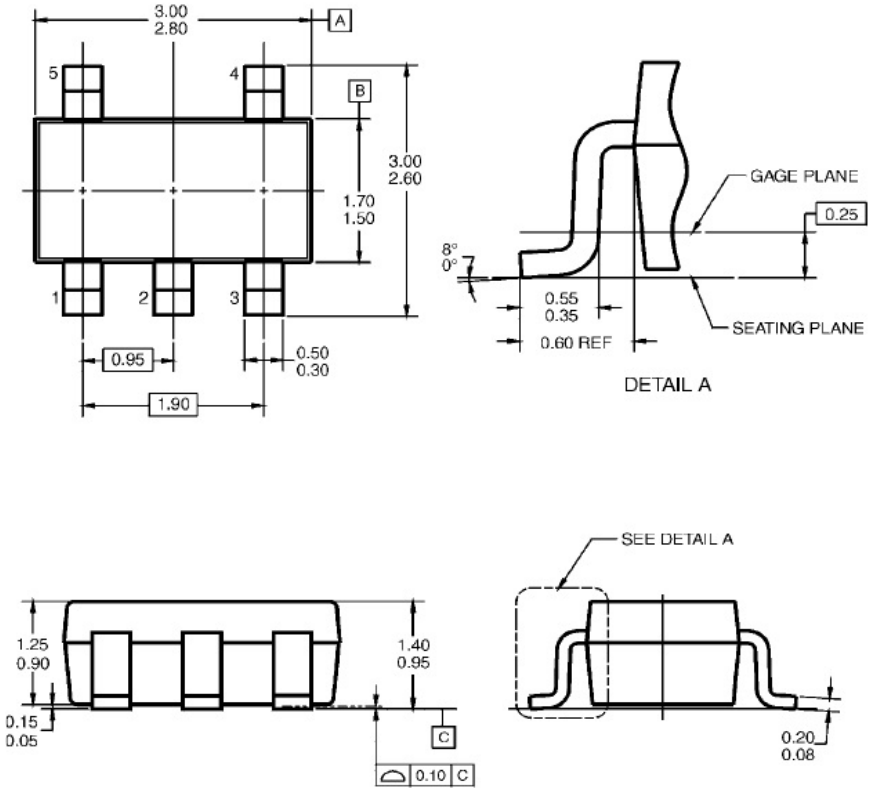


Fig 2. Ultralow noise adjustable regulator

Package Outline



LD Tech Corporation

Tel: +886-3-567-8806
Fax: +886-3-567-8706
E-mail: sales@ldtech.com.tw
Website: www.ldtech.com.tw