

Features

- Low Start-Up and Operating Current
- High Current Totem Pole Output
- Under voltage Lockout with Hysteresis
- Operating Frequency up to 500kHz

Applications

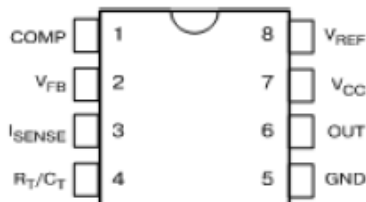
- PWM Controller Module

General Description

The LD6203 are fixed frequency current mode PWM controller. They are specially designed for OFF-Line and DC to DC converter applications with a minimal external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Protection circuitry includes built under voltage lockout and current limiting.

The LD6203 has UVLO thresholds of 16 V (on) and 10 V (off). It can operate within 100% duty cycle. The LD620x have 80 μ A (typ.) start-up current.

Package Pin Out



Ordering Information

		Packing Options	
Part No.	Package	Tube (TU)	Tape & Reel (TR)
LD6205	SOP-8	LD6205S1-TU	LD6205S1-TR

- Package material default is "Green" package.

Product Marking

LD8888	◇ Line 1 – "LD" is a fixed character
SSSSS...	8888: product name
●	◇ Line 2 – SSSSS...: lot number

Absolute Maximum Ratings

Parameter	Maximum	Unit
Supply Voltage (low impedance source)	30	V
Output Current	±1	A
Input Voltage (Analog Inputs Pins 2,3)	-0.3 to 5.5	V
Error Amp Output Sink Current	10	mA
Power Dissipation (T _A =25°C)	1	W
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering 5 sec.)	260	°C
Operating Temperature Range (T _J)	-40 to 125	°C
Min ESD rating (R=1.5k C=100pF)	2	KV

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics

V_{CC}=15V¹, R_T=10KΩ, C_T=3.3nF, T_J=-40°C to +125°C, unless otherwise specified

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reference Section						
Reference Output Voltage	V _{Ref}	T _J = 25°C, I _{Ref} = 1 mA	4.9	5.0	5.1	V
Line Regulation	ΔV _{Ref}	12V ≤ V _{CC} ≤ 25 V	–	6.0	20	mV
Load Regulation	ΔV _{Ref}	1 mA ≤ I _{Ref} ≤ 20 mA	–	6.0	25	mV
Short Circuit Output Current	I _{SC}	T _A = 25°C	–	-100	-180	mA
Oscillator Section						
Oscillation Frequency	f _{osc}	T _J = 25°C	47	52	57	KHz
Frequency Change with Voltage	Δf/ΔV _{CC}	12V ≤ V _{CC} ≤ 25 V	–	0.05	1.0	%
Oscillator Amplitude	V(osc)	(Peak to peak)	–	1.6	–	V
Discharge current	I _{DHC}	T _J = 25°C	7.5	8.5	9.5	V
Error Amplifier Section						
Input Bias Current	I _{Bias}	V _{FB} =3V	–	-0.1	-2	μA
Input Voltage	V _{I(EA)}	V _{pin1} =2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	A _{VOL}	2V ≤ V _o ≤ 4 V	65	90	–	dB
Unity Gain Bandwidth	UGBW	T _J = 25°C	0.5	1.0	–	MHz
Power Supply Rejection Ratio	PSRR	12V ≤ V _{CC} ≤ 25 V	60	70	–	dB
Output Sink Current	I _{sink}	V _{pin2} =2.7V, V _{pin1} =1.1V	2	7	–	mA
Output Source Current	I _{source}	V _{pin2} =2.3V, V _{pin1} =5V	-0.5	-1.0	–	mA
High Output Voltage	V _{OH}	V _{pin2} =2.3V, R _L =15KΩ to GND	5.0	7.0	–	V
Low Output Voltage	V _{OL}	V _{pin2} =2.7V, R _L =15KΩ to Pin8	–	0.8	1.1	V
Current Sense Section						
Gain ^{+2*3}	G _v	Note 1&2	2.85	3.0	3.15	V/V
Maximum Input Signal ⁺²	V _{I(Max)}	V _{Pin1} = 5V	0.9	1.0	–	V
			0.85	–	1.1	–
Supply Voltage Rejection ⁺²	SVR	12V ≤ V _{CC} ≤ 25V	–	70	–	dB
Input Bias Current	I _{Bias}	V _{pin3} =3v	–	-3.0	-10	μA
Output Section						
Low Output Voltag	V _{OL}	I _{sink} =20mA	–	0.08	0.4	V
		I _{sink} =200mA	–	1.4	2.2	–

High Output Voltage	V_{OH}	$I_{sink}=20mA$	13	13.5	–	V
		$I_{sink}=200mA$	12	13.0	–	
Rise Time ^{*4}	t_R	$T_J = 25^{\circ}C, C_L=1nF$	–	45	150	nS
Fall Time ^{*4}	t_F	$T_J = 25^{\circ}C, C_L=1nF$	–	35	150	nS
Undervoltage Lockout Section						
Start Threshold	$V_{TH(ST)}$	–	7.8	8.4	9.0	V
Min. Operating Voltage (After Turn On)	$V_{OPR(min)}$	–	7.0	7.6	8.2	V
PWM Section						
Max. Duty Cycle	$D_{(Max)}$	$T_J = 25^{\circ}C$	47	48	50	%
		$T_J = T_{low} \text{ to } T_{high}$	46	–	50	
Min. Duty Cycle	$D_{(Min)}$	–	–	–	0	%
Total Standby Current						
Start-Up Current	I_{ST}	–	–	0.080	0.14	mA
Operating Supply Current	$I_{CC(OPR)}$	$V_{pin3}=V_{pin2}=0V$	–	13	17	mA
Zener Voltage	V_Z	$I_{CC}=25mA$	30	38	–	V

Notes:

*1. Adjust VCC above the Start Threshold before setting it to 15V.

*2. The parameter measured at a trip point of a latch with $V_{Pin2}=0$.

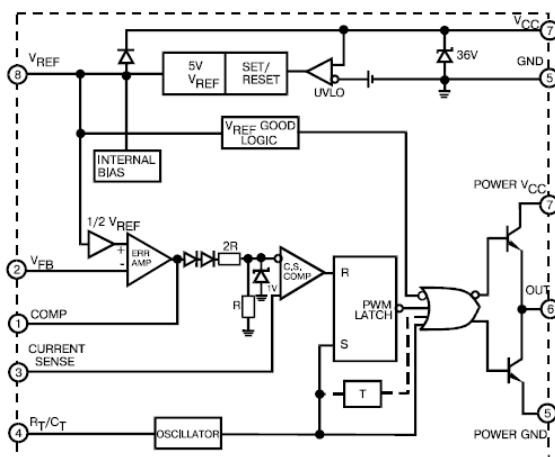
*3. Gain defined as $A= V_{Pin1}/V_{Pin3}$; $0 V \leq V_{Pin3} \leq 0.8V$.

*4. These parameters, although guaranteed, are not 100% tested in production.

Pin Description

Name	Description
COMP	This pin is the Error Amplifier output and is made for loop compensation.
VFB	This is an inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
ISENSE	A voltage proportional to an inductor current is applied to this input. The PWM uses this information to terminate the output switch conduction.
RT/CT	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to VREF and capacitor CT to ground.
GND	This pin is the combined control circuitry and power ground.
OUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
VCC	This pin is a positive supply of the integrated circuit.
VREF	This is a reference output. It provides charging current for capacitor CT through resistor RT

Block Diagram



Typical Application Circuit

APPLICATION INFORMATION

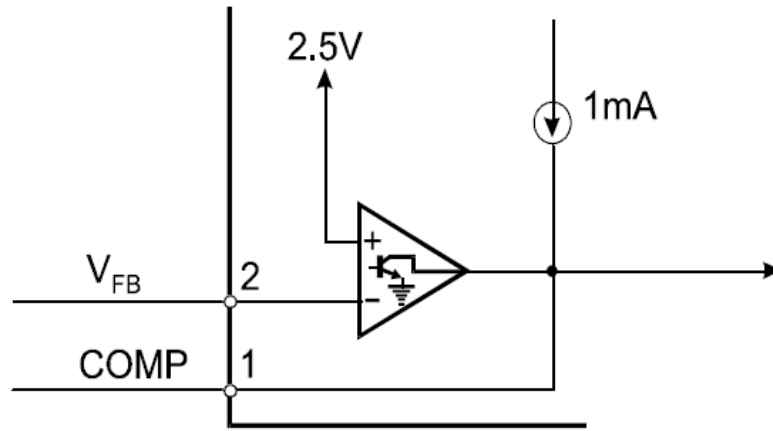


Fig.1. Error Amp Configuration

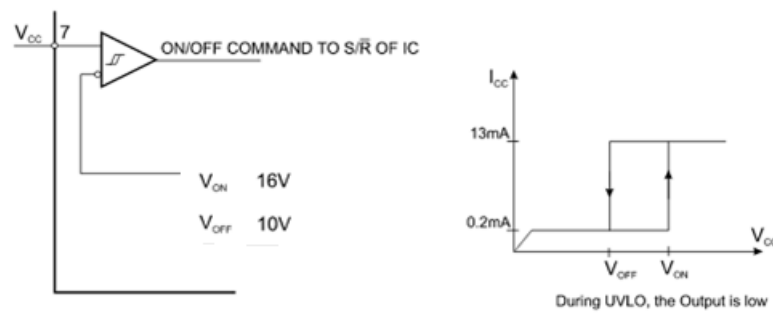


Fig.2. Undervoltage Lockout (UVLO)

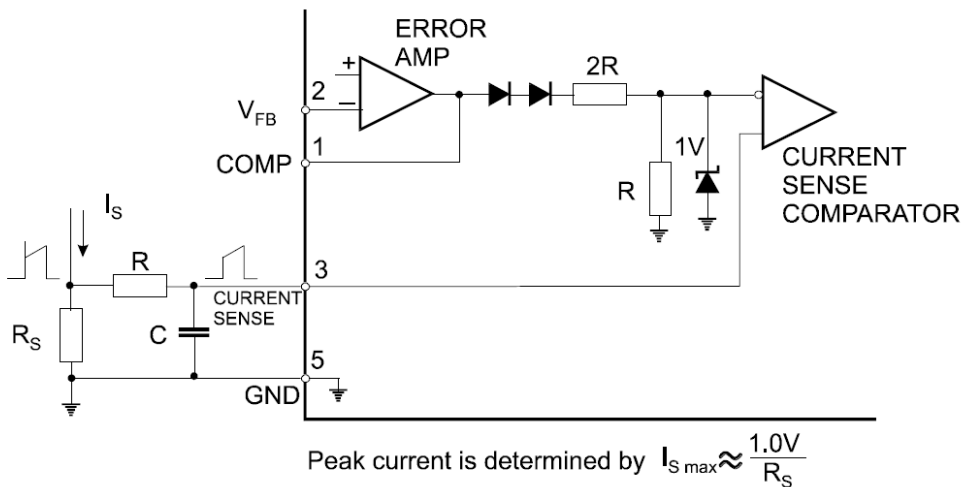


Fig.3. Current sense circuit

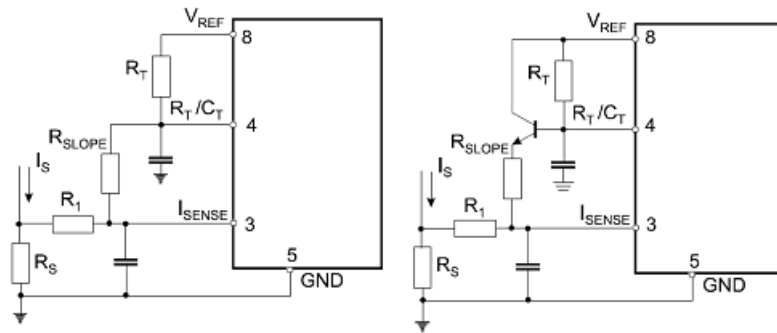
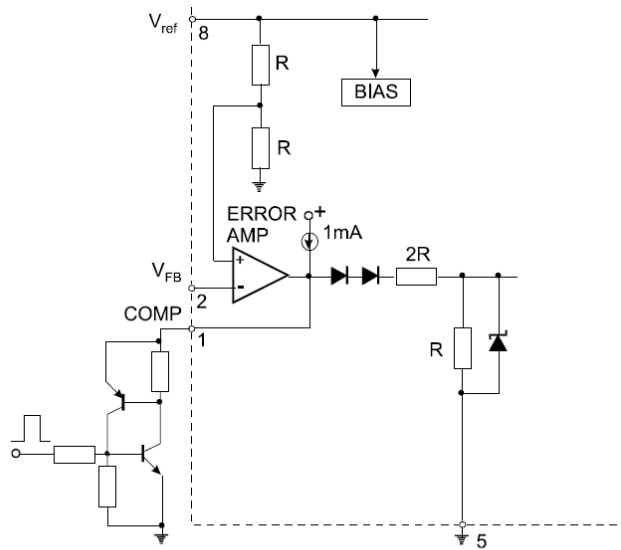


Fig.4. Slope compensation techniques



SCR must be selected for a holding current of less than 0.5mA.
The simple two-transistor circuit can be used in place of the SCR as shown

Fig.5. Latched shutdown

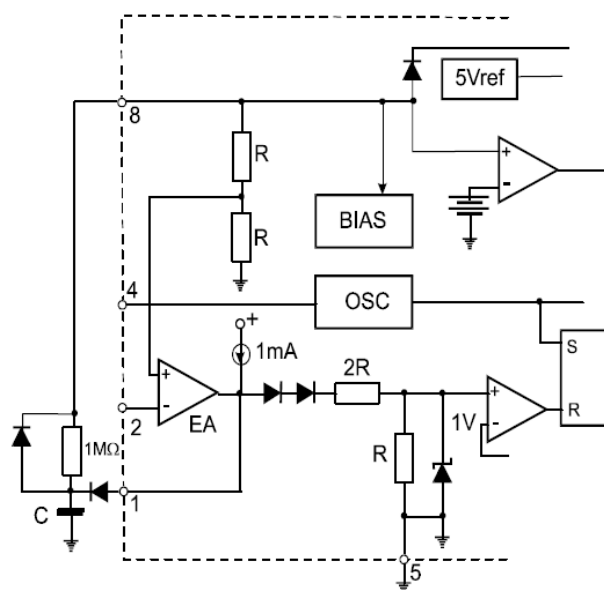
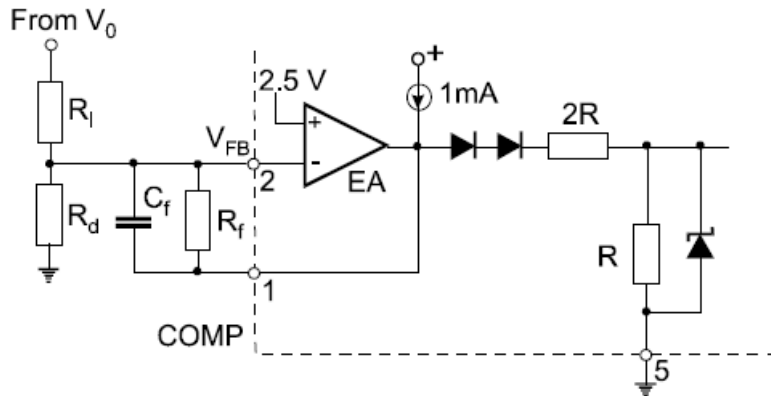
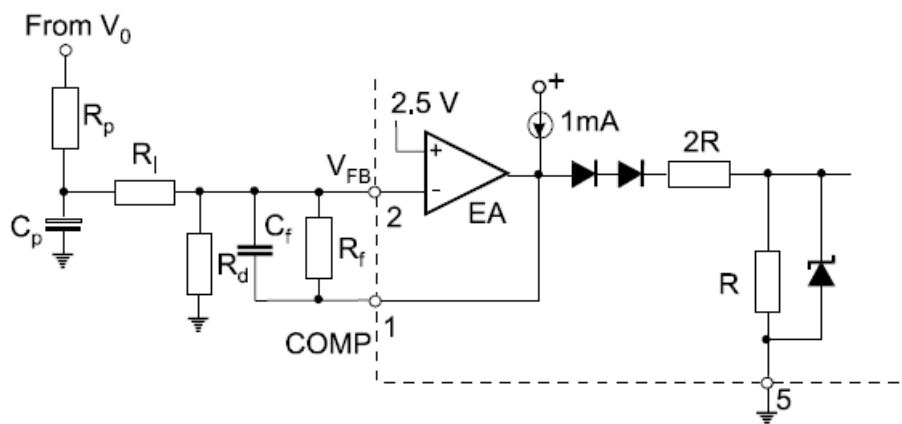


Fig.6. Soft-start circuit



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Fig.7. Error amplifier compensation

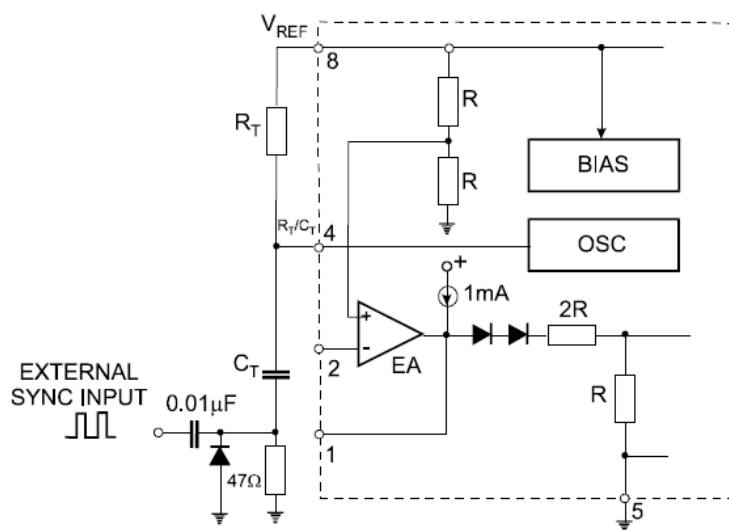


Fig.8. External clock synchronization

Typical performance Characteristics

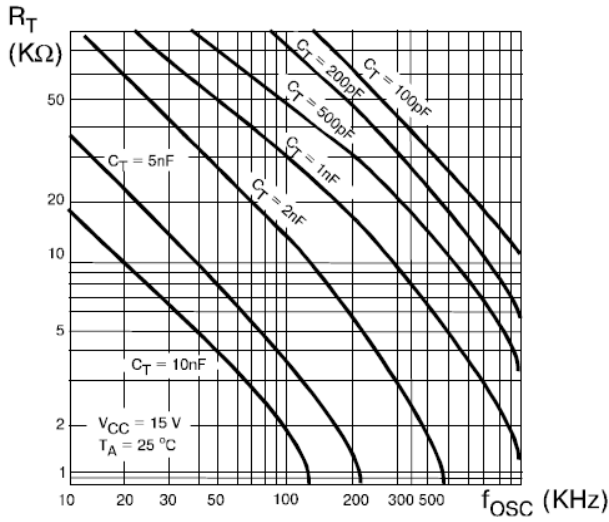


Figure 1 Timing Resistor vs. Oscillator Frequency

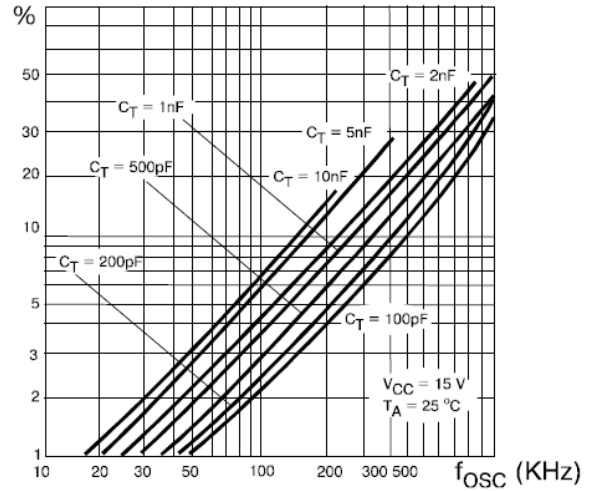


Figure 2 Output Dead-Time vs. Oscillator Frequency

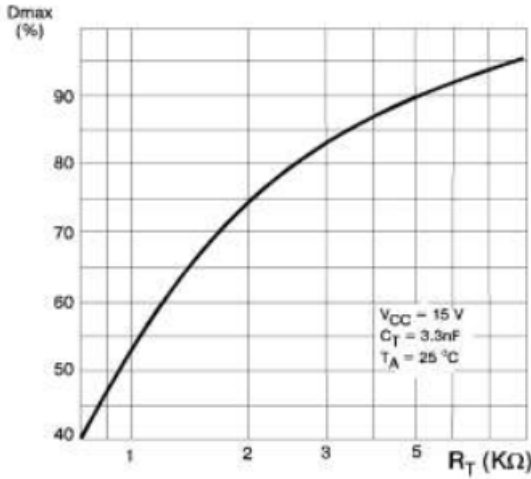


Figure 3 Maximum output duty cycle vs. Timing resistor

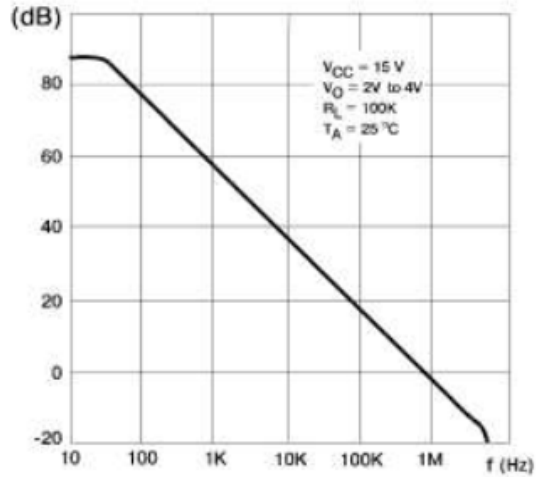


Figure 4 Error Amp Open-Loop Gain vs. Frequency

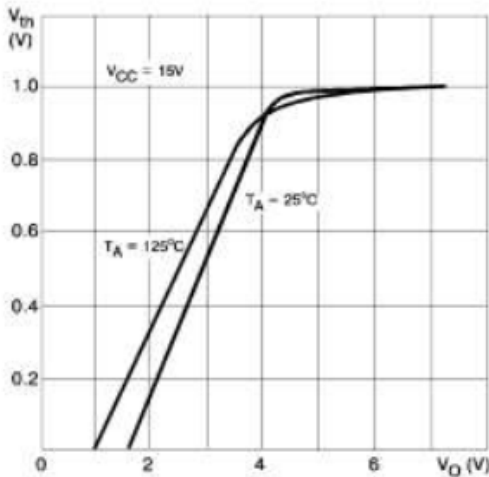


Figure 5 Current sense input threshold vs. Error amp output voltage

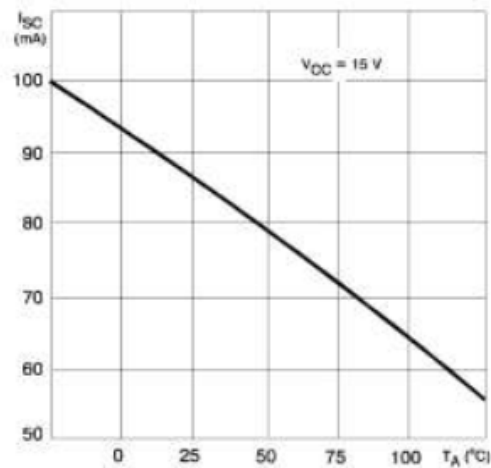


Figure 6 Reference Short Circuit Current vs. temperature

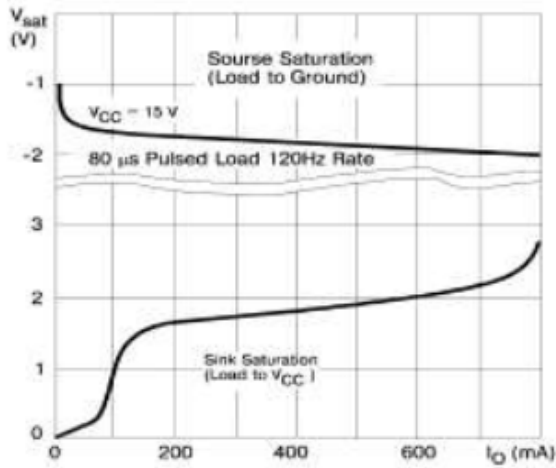


Figure 7 Output saturation voltage V.S. load current $T_A = 25^\circ\text{C}$

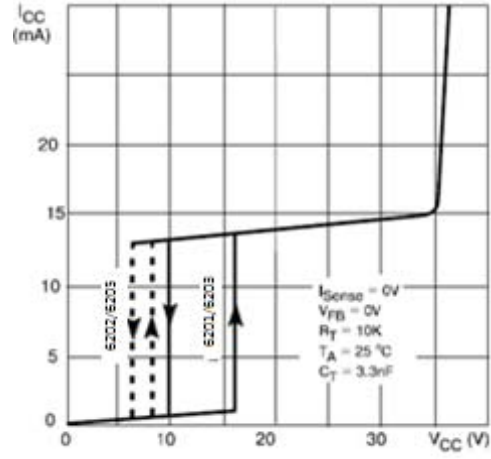


Figure 8 Supply current vs. supply voltage

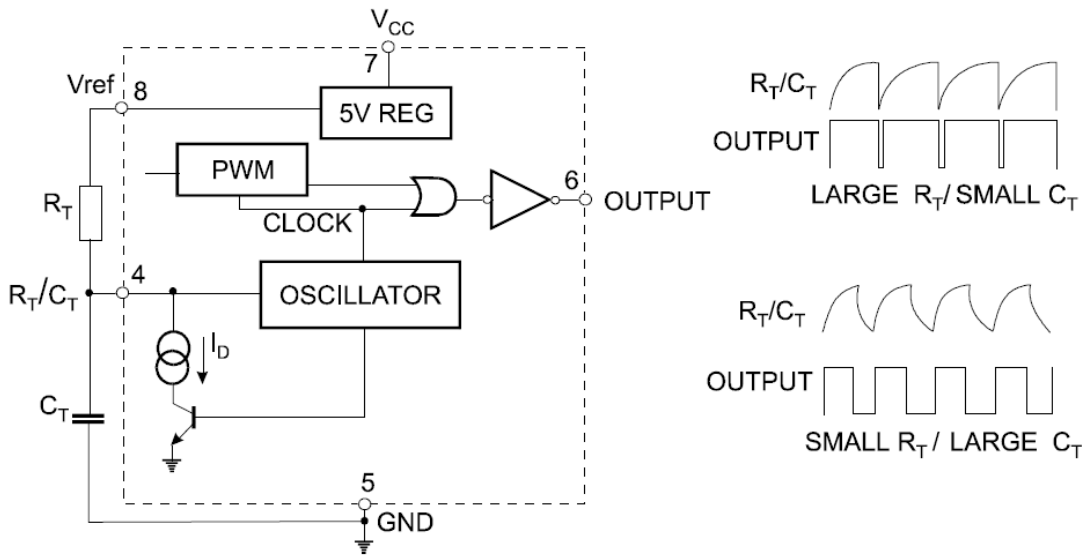
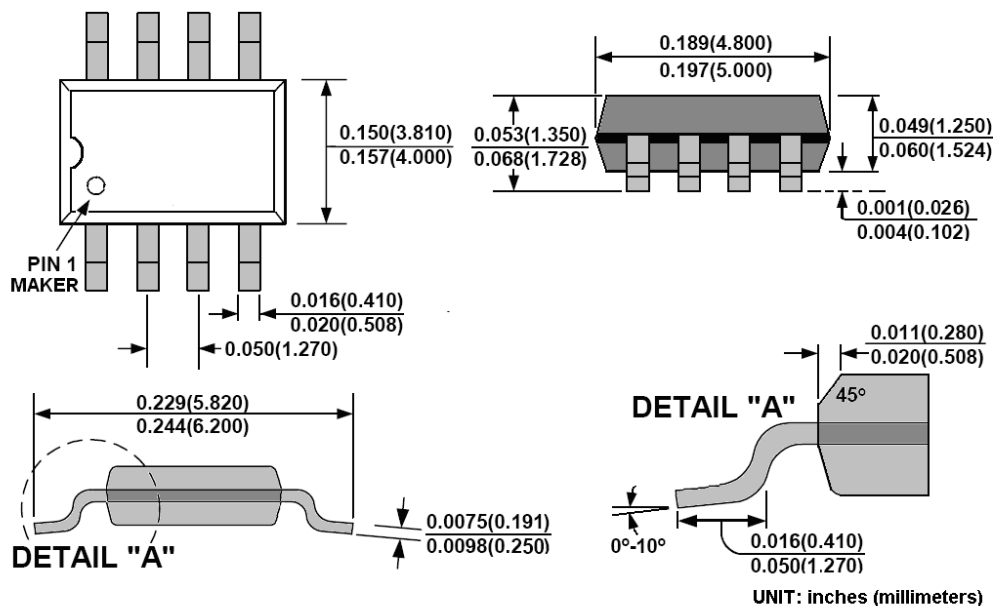


Figure 9 Oscillator and Output waveforms

Package Outline
SOP-8:



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